Penguin Edge™ MVME8100 Series

Installation and Use
P/N: 6806800P25P
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About this Manual

Overview of Contents

This manual provides the information required to install and configure the Penguin Solutions MVME8100, MVME8105 and MVME8110 boards. Additionally, this manual provides specific preparation and installation information and data applicable to the board.

The MVME8100 and MVME8105 are high-performance, dual core processor boards featuring the NXP$^{©}$ QorIQ$^{©}$ P5020 processor.

The MVME8110 is a high-performance, single core processor board featuring the NXP QorIQ P5010 processor.

This manual contains the following sections, chapters and appendices:

Abbreviations

This document uses the following abbreviations:

TERM	MEANING
ANSI	American National Standard Institute
CMC	Common Mezzanine Card
COP	Common On-chip Processor
CPLD	Complex Programmable Logic Device
CRC	Cyclic Redundancy Check
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
DMA	Direct Memory Access
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
eMMC	Enhanced Module Management Controller
FCC	Federal Communications Commission
FIFO	First In First Out
GMII	Gigabit Media Independent Interface
IEEE	Institute of Electrical and Electronics Engineers
I2C	Inter IC
IWD	Initial Hardware Watchdog
JTAG	Joint Test Access Group
LBC	Local Bus Controller
MRAM	Magnetoresistive random-access memory
OSWD	OS Watchdog
PCIE	Peripheral Component Interconnect Express
PCI-X	Peripheral Component Interconnect -X
PIC	Programmable Interrupt Controller
PIM	PCI Mezzanine Card Input/Output Module

TERM	MEANING
PMC	PCI Mezzanine Card
PLD	Programmable Logic Device
PrPMC	Processor PCI Mezzanine Card
QUART	Quad Universal Asynchronous Receiver/Transmitter
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real-Time Clock
RTM	Rear Transition Module
SATA	Serial AT Attachment
SBC	Single Board Computer
SDRAM	Synchronous Dynamic Random Access Memory
SELV	Safety Extra Low Voltage
SMT	Surface Mount Technology
SGMII	Serial Gigabit Media Independent Interface
SPD	Serial Presence Detect
SRAM	Static Random Access Memory
SRIO	Serial Rapid IO
TSEC	Three-Speed Ethernet Controller
2eSST	Two edge Source Synchronous Transfer
UART	Universal Asynchronous Receiver/Transmitter
VITA	VMEbus International Trade Association
VME	VMEbus (Versa Module Eurocard)
VPD	Vital Product Data
XMC	PCI Express Mezzanine Card

Conventions

The following table describes the conventions used throughout this manual.

Table P1   Conventions Table

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
Screen	Used for on-screen output and code related elements or commands. Sample of Programming used in a table (9pt)
Courier + Bold	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury

Table P1   Conventions Table (continued)

Notation	Description
	Indicates a property damage message
	Indicates a hot surface that could result in moderate or serious injury
	Indicates an electrical situation that could result in moderate injury or death
	Indicates that when working in an ESD environment care should be taken to use proper ESD practices
	No danger encountered, pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800P25P	July 2022	Rebrand to Penguin Solutions
6806800P25O	September 2018	Rebrand to SMART Embedded Computing.

About this Manual

Part Number	Publication Date	Description
6806800P25N	April 2019	Updated document template, minor grammar updates, converted list of product features to a comparison table. Changed Freescale to NXP in text and diagrams and figures where used. Removed Board Variants and Board Accessories tables; added references to product data sheets in the Related Documentation table (Appendix A). Updated Standard Compliances table.
6806800P25M	July 2016	Added a notice under Table 2-3 on page 45 and updated Table 1-1 on page 37.
6806800P25L	May 2016	Removed *Declaration of Conformity of MVME8100*, *Declaration of Conformity of MVME8105*, and *Declaration of Conformity of MVME8110*.
6806800P25K	October 2015	Changed as MVME8100/MVME8105/MVME8110.
6806800P25J	July 2015	Updated CPLD Tick Timer section.
6806800P25H	October 2014	Updated *Boot Options*.
6806800P25G	September 2014	Changed title as MVME8100 / MVME8110. Added information about MVME8110 and Declaration of Conformity.
6806800P25F	June 2014	Rebrand to Artesyn template.
6806800P25E	December 2013	Added chapter Boot System.
6806800P25D	September 2013	Updated Table 1-1, Table 1-2, Table 2-1, Table 2-3, PMC/XMC Installation, Table 3-2, and Table 3-5. Added Figure 2-2, SATA Installation, Figure 2-4, Figure 3-2, Interrupt Controller Assignments and GPIO Electrical Characteristics.
6806800P25C	December 2012	Updated Standard Compliances.
6806800P25B	November 2012	GA release.
6806800P25A	May 2012	First edition.

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Penguin Solutions™ intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Penguin Solutions representative.

This product is a Safety Extra Low Voltage (SELV) device designed to meet the EN60950-1 requirements for Information Technology Equipment. The use of the product in any other application may require safety evaluation specific to that application.

Only personnel trained by Penguin Solutions or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Penguin Solutions representative for service and repair to make sure that all safety features are maintained.

EMC

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. Changes or modifications not expressly approved by Penguin Solutions could void the user's authority to operate the equipment. Board products are tested in a representative

system to show compliance with the above mentioned requirements. A proper installation in a compliant system will maintain the required performance. Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained.

Warning! This is a Class A device. This device may cause radio interference in residential areas. In this case, the operator may be required to take appropriate measures.

Operation

Product Damage

High humidity and condensation on the board surface causes short circuits.

Do not operate the board outside the specified environmental limits.

Make sure the board is completely dry and there is no moisture on any surface before applying power.

Damage of Circuits

Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.

Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

Board Malfunction

Switches marked as reserved might carry production-related functions and can cause the board to malfunction if their setting is changed.

Do not change settings of switches marked as reserved. The setting of switches which are not marked as reserved has to be checked and changed before board installation.

Installation

Data Loss

Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

Make sure all software is completely shut down before removing power from the board or removing the board from the chassis.

Product Damage

Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Product Damage

Inserting or removing modules with power applied may result in damage to module components.

Before installing or removing additional devices or modules, read the documentation that came with the product.

Cabling and Connectors

Product Damage

RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

Battery

Board/System Damage

Incorrect exchange of lithium batteries can result in a hazardous explosion.

When exchanging the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models. If the respective battery model is not available, contact your local Penguin Solutions sales representative for the availability of alternative, officially approved battery models.

Data Loss

Exchanging the battery can result in loss of time settings. Backup power prevents the loss of data during exchange.

Quickly replacing the battery may save time settings.

Data Loss

If the battery has low or insufficient power the RTC is initialized.

Exchange the battery before seven years of actual battery use have elapsed.

PCB and Battery Holder Damage

Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

Environment

Improper disposal of used products may harm the environment. Always dispose of used products according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

Penguin Solutions™ ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem Produkt in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Penguin Solutions.

Das Produkt wurde entwickelt, um die Sicherheitsanforderungen für SELV Geräte nach der Norm EN 60950-1 für informationstechnische Einrichtungen zu erfüllen. Die Verwendung des Produkts in einer anderen Anwendung erfordert eine Sicherheitsüberprüfung für diese spezifische Anwendung.

Einbau, Wartung und Betrieb dürfen nur von durch Penguin Solutions ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Penguin Solutions. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

EMV

Das Produkt wurde in einem Penguin Edge™ Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produktes in Gewerbe- sowie Industriegebieten gewährleisten.

Das Produkt arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Wird das Produkt in einem Wohngebiet betrieben, so kann dies mit grosser Wahrscheinlichkeit zu starken Störungen führen, welche dann auf Kosten des Produktanwenders beseitigt werden müssen. Änderungen oder Modifikationen am Produkt, welche ohne ausdrückliche Genehmigung von Penguin Solutions durchgeführt werden, können dazu führen, dass der Anwender die Genehmigung zum Betrieb des Produktes verliert. Boardprodukte werden in einem repräsentativen System getestet, um zu zeigen, dass das Board den oben aufgeführten EMV-Richtlinien entspricht. Eine ordnungsgemässe Installation in einem System, welches die EMV-Richtlinien erfüllt, stellt sicher, dass das Produkt gemäss den EMV-Richtlinien betrieben wird. Verwenden Sie nur abgeschirmte Kabel zum Anschluss von Zusatzmodulen. So ist sichergestellt, dass sich die Aussendung von Hochfrequenzstrahlung im Rahmen der erlaubten Grenzwerte bewegt.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Betrieb

Beschädigung des Produktes

Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Produktes können zu Kurzschlüssen führen.

Betreiben Sie das Produkt nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Produkt kein Kondensat befindet.

Beschädigung von Schaltkreisen

Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.

Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Fehlfunktion des Produktes

Schalter, die mit Reserved gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.

Verstellen Sie nur solche Schalter, die nicht mit Reserved gekennzeichnet sind. Prüfen und ggf. ändern Sie die Einstellungen der nicht mit Reserved gekennzeichneten Schalter, bevor Sie das Produkt installieren.

Installation

Datenverlust

Das Herunterfahren oder die Deinstallation eines Boards bevor das Betriebssystem oder andere auf dem Board laufende Software ordnungsmemäss beendet wurde, kann zu partiellem Datenverlust sowie zu Schäden am Filesystem führen.

Stellen Sie sicher, dass sämtliche Software auf dem Board ordnungsgemäss beendet wurde, bevor Sie das Board herunterfahren oder das Board aus dem Chassis entfernen.

Beschädigung des Produktes

Fehlerhafte Installation des Produktes kann zu einer Beschädigung des Produktes führen.

Verwenden Sie die Handles, um das Produkt zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass das Face Plate oder die Platine deformiert oder zerstört wird.

Beschädigung des Produktes und von Zusatzmodulen

Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Produktes und der Zusatzmodule führen.

Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Kabel und Stecker

Beschädigung des Produktes

Bei den RJ-45-Steckern, die sich an dem Produkt befinden, handelt es sich entweder um Twisted-Pair-Ethernet (TPE) oder um E1/T1/J1-Stecker. Beachten Sie, dass ein versehentliches Anschließen einer E1/T1/J1-Leitung an einen TPE-Stecker das Produkt zerstören kann.

- Kennzeichnen Sie deshalb TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.
- Stellen Sie sicher, dass die Länge eines mit Ihrem Produkt verbundenen TPE-Kabels 100 m nicht überschreitet.
- Das Produkt darf über die TPE-Stecker nur mit einem Sicherheits-Kleinspannungs-Stromkreis (SELV) verbunden werden.

Bei Fragen wenden Sie sich an Ihren Systemverwalter.

Batterie

Beschädigung des Blades

Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.

Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde undbefolgen Sie die Installationsanleitung.

Datenverlust

Wenn Sie die Batterie austauschen, können die Zeiteinstellungen verloren gehen. Eine Backupversorgung verhindert den Datenverlust während des Austauschs.

Wenn Sie die Batterie schnell austauschen, bleiben die Zeiteinstellungen möglicherweise erhalten.

Datenverlust

Wenn die Batterie wenig oder unzureichend mit Spannung versorgt wird, wird der RTC initialisiert.

Tauschen Sie die Batterie aus, bevor sieben Jahre tatsächlicher Nutzung vergangen sind.

Schäden an der Platine oder dem Batteriehalter

Wenn Sie die Batterie mit einem Schraubendreher entfernen, können die Platine oder der Batteriehalter beschädigt werden.

Um Schäden zu vermeiden, sollten Sie keinen Schraubendreher zum Ausbau der Batterie verwenden.

Umweltschutz

Unsachgemäße Entsorgung von gebrauchten Produkten kann die Umwelt schädigen. Entsorgen Sie gebrauchte Produkte stets gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

Introduction

1.1 Overview

The MVME8100 single board computer is a VMEbus board based on the NXP® QorIQ® P5020 processor. It is a high performance 6U VME/VXS board targeted towards high-end military and industrial automation applications using VMEbus technology. The MVME8100 is compliant with the VMEbus International Trade Association (VITA) standards VMEbus, 2eSST, and PCI-X. The MVME8100 can accommodate two PCI/PCI Express Mezzanine Cards (PMC/XMC).

The MVME8105 is a dual core non-VXS version of the MVME8100 board based on the NXP QorIQ P5020 processor. It runs at 2.0GHz with 4GB DDR3. The MVME8105 provides a second 1000Base-TX RJ-45 interface on the front panel.

The MVME8110 is a single core non-VXS version of the MVME8100 board based on the NXP QorIQ P5010 processor. It runs at 1.2GHz with 2GB DDR3.

1.2 Feature Summary

The following table provides a summary of features for all three board variations. Not all processor features are implemented on the board.

Table 1-1   Board Feature Summary

Feature	MVME 8100	MVME 8105	MVME 8110
NXP® QorIQ®Processor	P5020 (1.8/2GHz)	P5020 (2.0GHz)	P5010 (1.2GHz)
e5500 cores	2	2	1
10GbE (XAIU) controllers	1	1	1
1GbE controllers (SGMII and RGMII)	5	5	5
64-bit DDR3/3L SDRAM memory controllers with ECC	2	2	1
Programmable Interrupt Controller (PIC)	Y	Y	Y
I^{2}C controllers	4	4	4
2-pin/4-pin UARTs	4/2	4/2	4/2
4-channel DMA engines	2	2	2
Enhanced local bus controller	1	1	1

Table 1-1   Board Feature Summary (continued)

Feature	MVME 8100	MVME 8105	MVME 8110
PCI Express 2.0 controller/ports	4	4	4
Serial Rapid IO controller/ports v1.3 compliant with features of v2.1)	2	2	2
Enhanced secure digital host controller (SD/MMC)	1	1	1
Enhanced Serial Peripheral Interfaces (eSPI with four chip selects)	1	1	1
High-speed USB 2.0 controllers with integrated PHYs	2	2	2
CoreNet platform cache with ECC	2Mbyte	2Mbyte	1Mbyte
SATA 2.0 controller	2	2	2
RAID5/6 engine	1	1	1
SEC encryption	Y	N	N
System Memory			
DDR3 SDRAM with ECC	4GB	4GB	2GB
DDR3 data rate	1333MT/s	1333MT/s	1200MT/s
SMBus			
512Kbit user configuration serial EEPROM	Y	Y	Y
256B serial presence detect (SPD) EEPROMs	Y	Y	Y
64Kbit Vital Product Data (VPD) EEPROM	Y	Y	Y
Real Time Clock (RTC) with battery backup**	Y	Y	Y
Temperature sensors	Y	Y	Y
RTM and XMC VPD EEPROMs	Y	Y	Y
Flash			
Soldered SPI Flash, 8MB each, switchable for uboot primary/backup support	2	2	2

Table 1-1   Board Feature Summary (continued)

Feature	MVME 8100	MVME 8105	MVME 8110
Hardware switch or software bit write protection for entire logical bank	Y	Y	Y
eMMC Flash	8GB	8GB	8GB
NVRAM			
Magneto resistive Random Access Memory (MRAM)	512KB	512KB	512KB
PCI Express			
4x ports to VXS backplane P0 (muxed with SRIO ports)	2	-	-
8x port to PMC/XMC Site 1	1	1	1
4x port to PMC/XMC Site 2	1	1	1
SRIO - 4x ports to VXS backplane P0 (muxed with PCIe ports)	2	-	-
USB			
USB 2.0 for front panel I/O	1	-	1
USB 2.0 for backplane RTM I/O	2	2	2
Ethernet			
10/100/1000BASE-T Ethernet port to front panel	1*	2	1
10/100/1000BASE-T Ethernet channels to P2/RTM	2	1	2
1000BASE-BX Ethernet SERDES channels to P0 backplane/RTM	2	-	-
SATA Ports			
SATA Gen 3 ports to P0 backplane/RTM	2	-	-
Serial Ports			
RS-232/422/485 console port to front panel or P2/RTM	1	1	1
RS-232/422/485 COM ports to P2/RTM	Up to 4	Up to 4	Up to 4

Table 1-1   Board Feature Summary (continued)

Feature	MVME 8100	MVME 8105	MVME 8110
VMEbus - VME64x and 2eSST	Y	Y	Y
Timers			
32-bit timers in CPU	8	8	8
Watchdog timer in CPU	Y	Y	Y
PMC/XMC sites with 64-bit PMCIO on Site 1	2	2	2
Option for 2.5" SATA SSD (PMC/XMC Site 2)	Y	Y	Y
GPIO Interface to RTM/P0	4	2	2
VXS Interface			
VITA 41 specification compliant	Y	Y	Y
Supports backplane P0 connector	Y	-	-
Form Factor			
Standard 6U, one slot	Y	Y	Y
Support 0.8 and 0.85 inch slot chassis	Y	Y	Y
Support heat frame on both sides for conduction cooled board	Y	Y	Y
Software Support			
VxWorks	Y	Y	Y
Linux	Y	Y	Y
Compatible with RTM (assembly # 0106852M***)	Y	Y	Y
I/O			
Micro DB-9 connector for console port on front panel	1*	1	1
USB 2.0 Type A connector on front panel	1*	-	1
Front panel RJ-45 connector with integrated LEDs for 10/100/1000 Ethernet channel	1*	2	1

Table 1-1   Board Feature Summary (continued)

Feature	MVME 8100	MVME 8105	MVME 8110
PMC/XMC Site 1 front I/O and rear PMC I/O	Y	Y	Y
PMC/XMC Site 2 front I/O	Y	Y	Y
Serial ports to P2/RTM, (two Micro DB-9 connectors on RTM panel and two on planar headers)	4	4	4
10/100/1000BASE-T Ethernet channels to RJ-45 connectors on RTM panel	2	1	2
1000BASE-BX Ethernet SERDES channels to backplane	2	-	-
USB 2.0 ports to RTM with USB Type A connectors on RTM panel	2	2	2
SATA port to RTM with eSATA connector on RTM	2	-	-
GPIOs to planar headers on RTM (**See note below**)	4	2	2
Other Features			
Front panel RESET switch	Y	Y	Y
LED front panel status indicators (four user/fail/ready LEDs)	Y	Y	Y
Planar status indicators	Y	Y	Y
Boundary scan support	Y	Y	Y

*Not present in ENP4 version

**Battery not present in ENP4 version

NOTE: The front panel I/O connectors are available only in ENP1 (air cooled variants). I/O signals in the ENP4 (conduction cooled) variant are accessed through P2 only.

1.3 Ordering and Support Information

Refer to the data sheets for the MVME81xx series of boards for a complete list of available variants and accessories. Refer to Appendix B or consult your local Penguin Solutions sales representative for the availability of other variants.

For technical assistance, documentation, or to report product damage or shortages, contact your local Penguin Solutions sales representative or visit https://www.penguinsolutions.com/edge/support//

1.4 Standard Compliances

The MVME8100 Series is designed to be CE compliant and to meet the following standard requirements.

Table 1-2   Board Standard Compliances

Standard	Description
UL 60950-1 EN 60950-1 IEC 60950-1 CAN/CSA C22.2 No 60950-1	Safety Requirements (legal)
CISPR 22 EN 55022 EN 55024 FCC Class A VCCI Japan AS/NZS CISPR 22	EMC requirements (legal) on system level (predefined Penguin Solutions system)
ETSI EN 300 019 series	Environmental Requirements
Directive (EU) 2015/863 (amending Annex II to Directive 2011/65/EU)	Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS). The MVME8100-202180404 ENP4 version is not RoHS compliant. It was compliant with RoHS 5 of 6 until the exemption expired in 2016. Customers may still purchase the non-RoHS product (with a waiver) for use in applications excluded from RoHS compliance.

1.5   Mechanical Data

The MVME8100 is a full 6U board with added mounting holes to support an ENP4 board variant. The MVME8100 Series occupies a single VME card slot.

The following table provides detailed mechanical data information.

Table 1-3   Mechanical Data

Characteristic	Value
Height	233.44mm (9.2 inches)
Depth	160.0mm (6.3 inches)
Front Panel Height	261.8mm (10.3 inches)
Width	19.8mm (0.8 inches)
Maximum Component Height	14.8mm (0.58 inches)
Weight (estimated)	0.58Kg (ENP1) 0.90Kg (ENP4)

Hardware Preparation and Installation

2.1   Overview

This chapter provides startup and safety instructions related to this product, hardware preparation instruction that includes default switch settings. System considerations and installation instructions for the baseboard, PMC, XMC, and Rear Transition Module (RTM) are also described in this chapter.

A fully implemented MVME8100 board consists of the baseboard plus:

- Two single-wide or one double-wide PCI Mezzanine Card (PMC) slot for added versatility.
- One rear transition module for support of the mapped I/O from the Product Name Short baseboard to the P2 connector.

NOTE: RTM is not applicable to the ENP4 version.

- Up to two optional XMC cards (in place of PMC modules).

Following are the steps to be performed before using the board. Be sure to read the entire chapter, including all caution and warning notes, before you begin.

1. Unpack the hardware. *Unpacking and Inspecting the Board on page 34*.
2. Configure the hardware by setting jumpers on the board and RTM. *Configuring the Board on page 38*.
3. Install the MVME8100 RTM (VXS1-RTM1) or the MVME8110 RTM (MVME8110-RTM) in the chassis. *Rear Transition Module on page 41*.
4. Install PMC module (if required). *Installing Accessories on page 41*.
5. Install XMC module (if required). *Installing Accessories on page 41*.
6. Install the MVME8100 board in the chassis. *Installing and Removing the Board on page 47*.
7. Attach cabling and apply power. *Completing the Installation on page 48*.
8. Install PIM on transition module (if required). Refer to the *VXS1-RTM1and MVME8110-RTM Installation and Use* manual.
9. Examine and/or change environmental parameters. *MVME8100 Series Single Board Computer Programmer's Reference*.
10. Program the board as needed for your applications. *MVME8100 Series Single Board Computer Programmer's Reference.*

2.2   Unpacking and Inspecting the Board

Read all notices and cautions prior to unpacking the product.

Use ESD protection	**Damage of Circuits** **Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.** **Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.**

Shipment Inspection

To inspect the shipment, perform the following steps:

1. Verify that you have received all items of your shipment:

    – MVME8100 board

    – Quick Start Guide

    – Safety Notes Summary

    – Any optional items ordered

2. Check for damage and report any damage or differences to customer service.

3. Remove the desiccant bag shipped together with the board and dispose of it according to your country's legislation.

Important Information	**The product is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, contact customer service immediately.**

2.3 Requirements

Make sure that the board, when operated in your particular system configuration, meets the requirements specified in the next sections.

2.3.1 Environmental Requirements

The following table lists the currently available specifications for the environmental characteristics of the MVME8100. A complete functional description of the MVME8100 baseboard appears in Chapter 4 .

The MVME8100 has ENP1 and ENP4 variants which comply with the following environmental and regulatory specifications.

The MVME8105 has ENP1variant only which comply with the following environmental and regulatory specifications.

The MVME8110 has ENP1variant only which comply with the following environmental and regulatory specifications.

Important Information	**For ENP1 boards, the operating temperatures refer to the temperature of the air circulating around the board and not to the component temperature.**
	For ENP4 board, the operating temperature refers to the temperature at the card edge frame.

Table 2-1   MVME8100 Series Specifications

Characteristics	ENP1	ENP4
Cooling Method	Forced Air	Conduction
Operating temperature	0°C to +55°C	–40°C to +85°C

Table 2-1   MVME8100 Series Specifications (continued)

Characteristics	ENP1	ENP4
Storage Temperature	-40° C to +85° C	-55°C to +105°C **Note**: The MVME8100 ENP 4 version includes NAND Flash memory in the form of the eMMC. The specified storage limits for the MVME8100 ENP 4 version are -55°C to +105°C. It should be noted that the industry standard (for Flash) as well as the specific vendor of this component only warrants performance (without data degradation) from -40°C to +85°C. Storage of the MVME8100 outside this range (while supported by other components on the board) may result in an unspecified reduction in the data retention capabilities of the eMMC.
Relative humidity	To 95% RH	To 100% RH
Vibration Sine (10min/axis)	2G, 5 to 500Hz	10G, 15 to 2000Hz
Vibration Random (1hr/axis)	$0.002g^2$/Hz, 15 to 2000Hz[1] (2G RMS)	$0.1g^2$/Hz, 15 to 2000Hz (12GRMS)[2]
Shock	20g/11mS	40g/11mS
Conformal Coating	No	Option (Acrylic)

Product Damage

High humidity and condensation on the board surface causes short circuits.

Do not operate the board outside the specified environmental limits.

Make sure the board is completely dry and there is no moisture on any surface before applying power.

2.3.2   Power Requirements

The MVME8100 Series uses the backplane +5V source to power each on board power supply. The +3.3V backplane supply is not utilized in order to have backward compatibility with old 3-row chassis. The -12V and +12V is routed through to the XMC and PMC connectors. The power estimates provided in the following table is the total board consumption from +5V, excluding the PMC/XMC, SATA HDD/SSD and USB devices.

Table 2-2   Operating Voltages

Voltages	Minimum	Normal	Maximum
+5.0V	4.875V (-2.5%)	5.0V	5.25V (+5%)

Table 2-3   Power Requirements

Board Variant	Power
MVME8100-202200401S/E MVME8105-01E MVME8110-01S/E (ENP1)	Board idle at OS prompt: 38 Watts, typical Operating load*: 42 Watts, typical 54 Watts, Max(@55°C) *Operating conditions: No RTM, PMC/XMC or peripherals.
MVME8100-202180404 (ENP4)	Operating load*: 65 Watts, max (@ 85°C card edge temperature)

> **Important Information**
>
> **The MVME8100-202180404 is non-compliant with the EU RoHS Directive and the CE mark as of July 21, 2016.**

The following table shows the power limits due to the available 5 volts pins, when the MVME8100/MVME8105 is installed in either a 3-row or 5-row chassis and when PMCs/XMCs are present.

Chassis Type	Power Limit	Power limits PMCs or XMCs
3-Row	70W maximum	Below 70W[1]
5-Row	90W maximum	Below 90W[1]

1. Keep below power limit. Cooling limitations must be considered.

2.3.3   Thermal Requirements

The MVME8100 Series boards requires a minimum air flow of 10CFM uniformly distributed across the board, with the airflow traveling in the direction from PMC/XMC 1 to PMC/XMC 2, when operating at a 55°C (131°F) ambient temperature.

2.3.4   Thermally Significant Components

The chassis into which the MVME8100 Series boards are installed must provide sufficient airflow to maintain proper board operating temperature. The P5020/P5010 processor temperature should be monitored while the board is operational to ensure that the processor core temperature does not exceed 100°C. The processor core temperature can be read using the I^2C sensor at address 0x4C on the processor I^2C bus #1. For more information, refer *MVME8100/MVME8105/MVME8110 Single Board Computer Programmer's Reference*.

2.3.5   Equipment Requirements

The following equipment is recommended to complete a system using an MVME8100, MVME8105 or MVME8110 board:

- VMEbus system enclosure
- System console terminal
- Operating system (and/or application software)

2.4   Configuring the Board

The board provides software control over most options. Settings can be modified to fit the user's specifications. To configure, set the bits in the control register after installing the board in a system. Make sure that all user-defined switches are properly set before installing a PMC/XMC module. For more information about switches, see *Switches on page 72*.

Prior to installing PMC modules on the baseboard, ensure that all switches that are user configurable are set properly. Refer to *Figure 2-1* or the board itself, for the location of specific switches and set the switches according to the descriptions provided in *Configuration Switches on page 73*.

Figure 2-1   Switch Locations (ENP1 board)
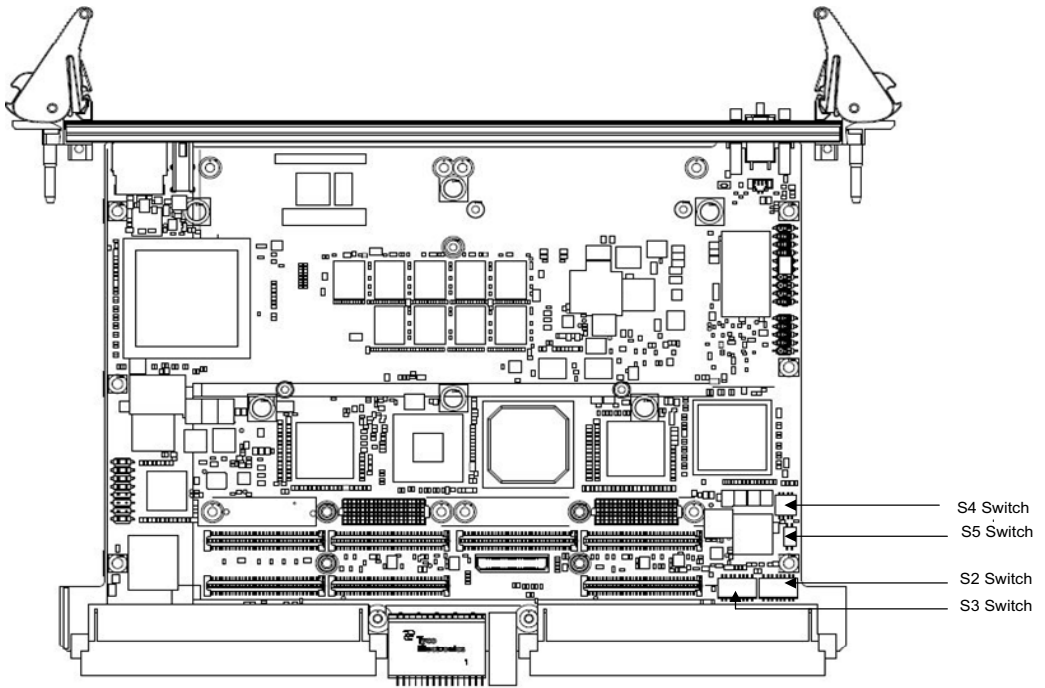
Figure 2-2   Switch Locations (ENP4 Board)
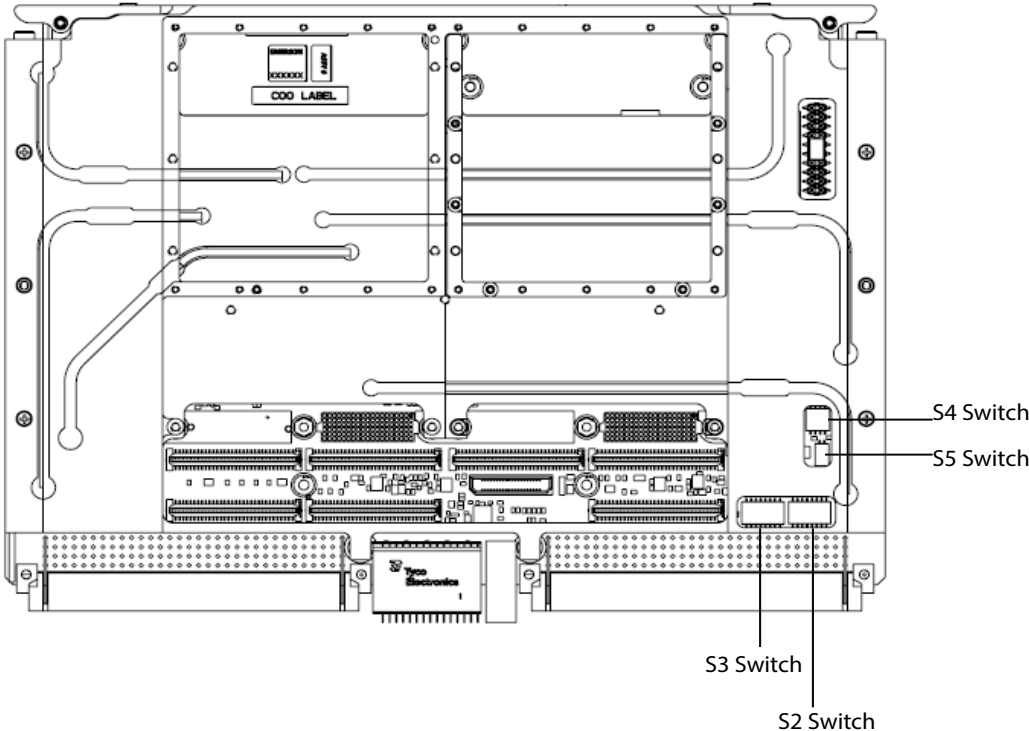
2.5 Installing Accessories

This section describes the procedures for installing the RTM, PMCs, and the XMCspan on the baseboard.

2.5.1 Rear Transition Module

The RTM of MVME8100 Series does not support hot swap. You must remove power to the system before installing the module. Before installing the transition module, you may need to manually configure the RTM switches and install a PMC I/O Module (PIM).

Use ESD protection	**Damage of Circuits** **Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.** **Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.**

⚠	**Product Damage** **Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.**

⚠	**Board Malfunction** **Switches marked as reserved might carry production-related functions and can cause the board to malfunction if their setting is changed.** **Do not change settings of switches marked as reserved. The setting of switches which are not marked as reserved has to be checked and changed before board installation.**

Installation Procedure

To begin the installation of the RTM in a chassis, proceed as follows:

1. Turn all equipment power OFF and disconnect the power cable from the AC power source.

2. Remove the chassis cover as instructed in the equipment user's manual.

3. Remove the filler panel(s) from the appropriate card slot(s) at the rear of the chassis (if the chassis has a rear card cage).

4. Install the top and bottom edge of the RTM into the rear guides of the chassis.

5. Ensure that the levers of the two injector/ejectors are in the outward position.

6. Slide the RTM into the chassis until resistance is felt.

7. Simultaneously move the injector/ejector levers in an inward direction.

8. Verify that the RTM is properly seated and secure it to the chassis using the two screws located adjacent to the injector/ejector levers.

9. Connect the appropriate cables to the RTM.

Removal Procedure

1. Turn off the power.

2. Disconnect all the cables.

3. Loosen and remove the screws located adjacent to the injector/ejector levers that securing board to the chassis.

4. Move the injector/ejector levers in an outward direction.

5. Hold top and bottom edges of the board and exert minimal force when pulling the board from the chassis to prevent pin damage.

6. Remove the transition module from the chassis and insert the filler panels.

2.5.2   PMC/XMC Installation

The PMC connectors are placed to support two single-width PMCs or one double-width PMC. PMC site 1 supports front PMC I/O and rear PMC I/O via the Jn4 connector. PMC 1 I/O is routed to the VME P2 connector. PMC site 2 only supports front PMC I/O and does not have a Jn4 connector. The PMC 1 Jn4 user I/O signals only support low-current, high-speed signals and thus do not support current-bearing power supply usage.

The user-configured switches are accessible with the PMC/XMCs installed. The on-board PMC sites are configured to support +3.3V I/O PMC modules. The on-board PMC sites do not support +5.0V I/O PMC modules.

The MVME8100 ENP4 version only supports rugged conduction cooled PMC/XMC modules (see VITA 20-2001 for conduction cooled PMC for mechanical definition.

Follow the steps to install a PMC/XMC module onto the base board.

Installation Procedure

Read all notices and follow the steps to install a PMC/XMC on the baseboard.

Use ESD protection	**Damage of Circuits** **Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.** **Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.**

⚠	**Product Damage** **Inserting or removing modules with power applied may result in damage to module components.** **Before installing or removing additional devices or modules, read the documentation that came with the product.**

<div style="border:1px solid">

NOTICE

Logic Ground to Chassis Ground Isolation

The MVME8100 Series heat frames are isolated from the board logic ground. Installing a PMC or XMC module which has mounting locations connected to the module logic ground will result in a short between chassis ground and the MVME8100 Series logic ground.

</div>

1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis as a ground. Make sure that it is securely fastened throughout the procedure.

2. If the PMC/XMC has a front filler panel, remove the PMC/XMC filler plate from the front panel cut-out.

3. Remove the two rear stand-offs from the PMC/XMC. The heat frame of the Product Name Short has built-in rear stand-offs.

4. Slide the front bezel of the PMC/XMC into the cut-out from behind. The front bezel of the PMC/XMC module will be flushed with the board when the connectors on the module align with the mating connectors on the board.

NOTE: ENP4 PMC/XMC modules do not have front bezels.

5. Align the mating connectors properly and apply minimal pressure to the PMC/XMC until it is seated to the board.

6. Insert the two front PMC/XMC mounting screws through the mounting holes on the bottom side of the board, and then install the top side screws. Tighten the screws.

NOTE: Rugged PMC/XMC modules installed on an ENP4 MVME8100 have more than four mounting screws.

7. Install the board into the appropriate card slot. Make sure that the board is well seated into the backplane connectors. Do not damage or bend connector pins.

8. Replace the chassis or system cover.

9. Reconnect the system to the power source and then turn on the system.

Figure 2-3 Typical Placement of a PMC/XMC Module on a VME Module
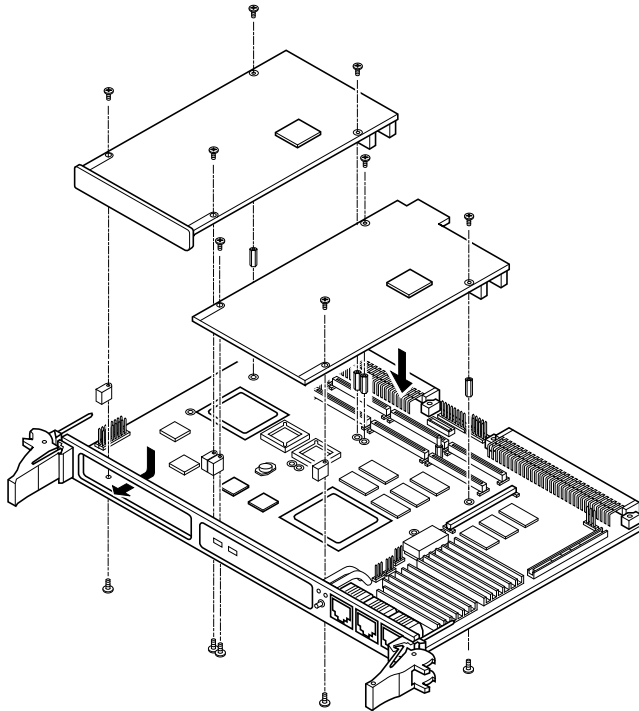
2.5.3   SATA Installation

A 2.5" SATA drive can be installed in PMC/XMC Site 2. The MVME8100-HDMTKIT4 SATA mounting kit (6706881A01x) provides the mounting hardware. A SATA drive which meets the intended board operating environment for temperature and vibration must be used.

Read all notices and follow the steps to install a SATA drive on the baseboard.

Use ESD protection	**Damage of Circuits**
	Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
	Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

⚠	**Product Damage**
	Inserting or removing modules with power applied may result in damage to module components.
	Before installing or removing additional devices or modules, read the documentation that came with the product.

NOTICE
Logic Ground to Chassis Ground Isolation
The MVME8100 Series heat frames are isolated from the board logic ground. Installing a PMC or XMC module which has mounting locations connected to the module logic ground will result in a short between chassis ground and the MVME8100 Series logic ground.

Figure 2-4   SATA Drive Installation
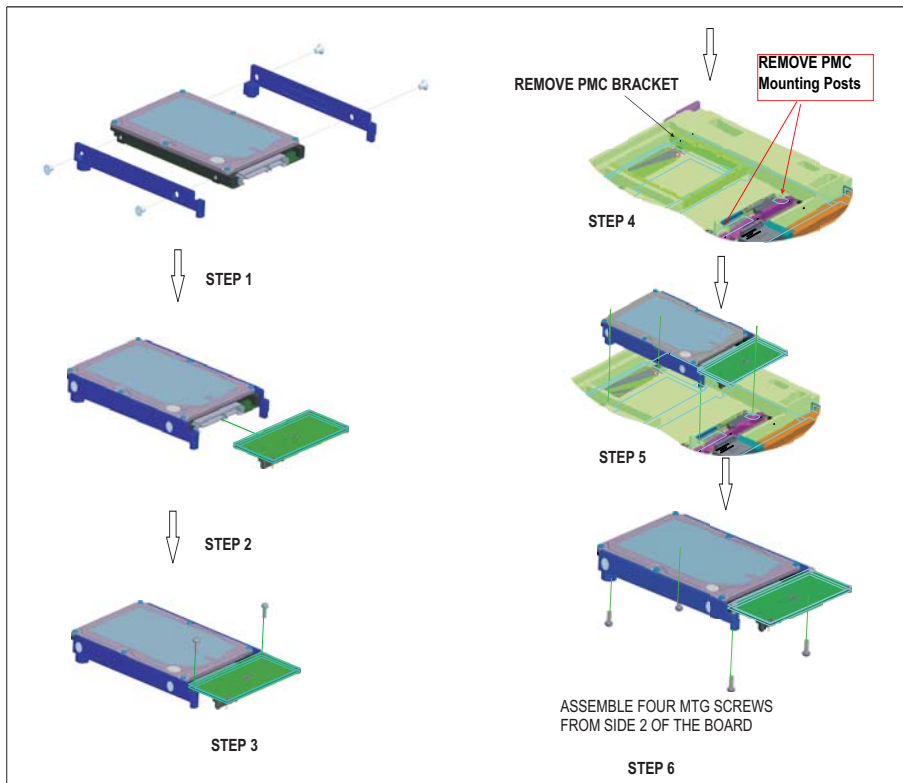
Use the following steps to install a SATA drive:

1. Wear an ESD strap to your wrist and fix the other end of the ESD strap to an electrical ground.

2. Secure mounting brackets to each side of SATA drive as shown in step 1 of *Figure 2-4*.

3. Attach SATA adapter board to SATA drive as shown in step 2 of *Figure 2-4*.

4. Use two screws to secure adapter to mounting brackets as shown in step 3 of *Figure 2-4*.

5. Remove PMC/XMC bracket and mounting posts from site 2 as shown in step 4 of *Figure 2-4*.

6. Attach SATA drive assembly with adapter board and mounting brackets to the board at PMC/XMC Site 2 as shown in step 5 of *Figure 2-4*. Make sure that the SATA adapter connector is fully mated with the board SATA connector.

7. Secure SATA drive assembly to board using four screws inserted from the bottom side of the board as shown in step 5 of *Figure 2-4*.

2.6   Installing and Removing the Board

This section describes the recommended procedure for installing the MVME board in a chassis.

The MVME8100 Series do not support hot swap, you must remove power to the slot or system before installing the module.

Before installing the board, ensure that the serial ports and switches are properly configured.

Installation Procedure

Before you install your module, please read all cautions, warnings and instructions presented in this section.

Use ESD protection	**Damage of Circuits**
	Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.
	Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

⚠	**Product Damage**
	Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

Use the following steps to install the MVME8100/MVME8105/MVME8110 into your computer chassis:

1. Wear an ESD strap on your wrist.

2.   Attach the other end of the ESD strap to an electrical ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.

3. Remove any filler panel that might fill the slot.

4. Install the top and bottom edge of the board into the guides of the chassis.

5. Ensure that the levers of the two IEEE locking injector/ejectors (if equipped)

6. are in the unlocked outward position.

7. Slide the board into the chassis until you feel resistance.

8. Simultaneously move the injector/ ejector levers (if equipped) in an inward direction until locked. If fitted with SCANBE ejectors, adjust them inward and apply pressure to them to seat the board.

9. Verify that the board is properly installed and secure it to the chassis using the two screws located adjacent to the injector/ejector levers.

10. When installing an ENP4 version board, the maximum torque that should be used on the wedge lock screws is 6 in-lbs.

11. Connect the appropriate cables to the board.

When the MVME8100 Series (and optionally, an RTM) is installed in a chassis, you are ready to connect peripherals and apply power to the slot or system.

The front-panel Micro DB-9 connector provides a console interface to U-boot. It presents an RS-232 DTE interface (TX/RX/CTS/RTS). The default serial configuration is 9600/8/N/1. This mates with an ITT MDSM-9SC-Z11 (or equivalent). The Penguin Solutions part number SERIAL-MINI-D2 converts this to a standard male DB-9 interface.

Removal Procedure

1. Turn off the power.

2. Disconnect all the cables.

3. Press the locking tabs (IEEE handles only) to eject the board.

4. Loosen and remove the screws adjacent to the injector/ejector levers that securing the module to the chassis.

5. Move the injector/ejector levers in outward direction.

6. Hold top and bottom edges of the board and exert minimal force when pulling the board from the chassis to prevent pin damage.

7. Carefully remove the board from the chassis and store the board in anti-static envelope.

2.7　Completing the Installation

The MVME8100 Series are designed to operate as an application-specific compute blade or an intelligent I/O board/carrier. It can be used in any slot in a VME chassis. When the board is installed in a chassis, you are ready to connect peripherals and apply power to the board.

Figure 3-1 on page 51 show the locations of the various connectors on the board.

> ⚠️ **Product Damage**
>
> **RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.**
>
> **Make sure that TPE connectors near your working area are clearly marked as network connectors.**
>
> **Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.**
>
> **Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).**
>
> **If in doubt, ask your system administrator.**

The console settings for the MVME8100 Series are:

- Eight bits per character
- One stop bit per character
- Parity disabled (no parity)
- Baud rate of 9600 baud

Verify that hardware is installed and the power/peripheral cables connected are appropriate for your system configuration.

Replace the chassis or system cover, reconnect the chassis to the AC or DC power source, and turn the equipment power on.

Connectors, LEDs, and Switches

3.1 Overview

This chapter summarizes the front panel connectors, LEDs, and on-board switches and their configuration for the MVME8100 Series board.

3.2 Front Panel

The following figures illustrate the location of the components available on the front panels.

Figure 3-1   MVME8100 - ENP1 Board Connectors, LEDs, Switches

Figure 3-2   MVME8100 - ENP4 LEDs and Switches
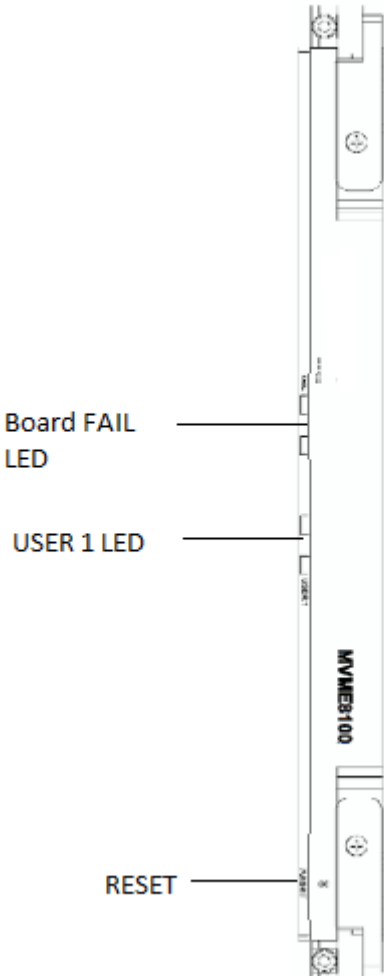
Figure 3-3   MVME8105 - ENP1 Board Connectors, LEDs, Switches
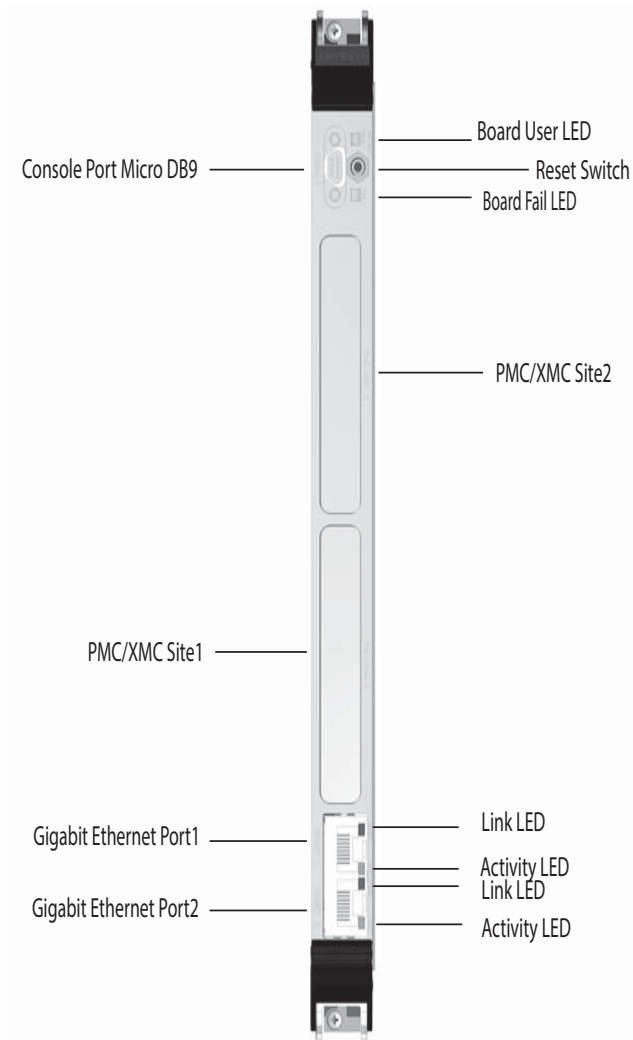
3.3   Connectors

This section describes the pin assignments and signals for the connectors on the MVME8100 Series boards.

3.3.1   External Connectors

3.3.1.1   Front Panel Connectors

The following are the front panel connectors:

- Serial console port (J1)
- Front panel Ethernet connector (J1)
- USB connector (J5)

Table 3-1   Console Front Panel Connector (J1)

Pin Number	RS-232 SIGNALING	RS-485 SIGNALING
1	NC	NC
2	COM_0_RX	COM_0_RX-
3	COM_0_TX	COM_0_TX-
4	NC	NC
5	GND	GND
6	NC	NC
7	COM_0_RTS	COM0_TX+
8	COM_0_CTS	COM0_RX+
9	NC	NC

Table 3-2   Front Panel Tri-Speed Ethernet Connector (J4)

NOTE: J4 is assembled only on ENP1	
Pin Number	**Signal Description**
1	VCC
2	TD0+
3	TD0-

Table 3-2   Front Panel Tri-Speed Ethernet Connector (J4) (continued)

NOTE: J4 is assembled only on ENP1	
Pin Number	**Signal Description**
4	TD1+
5	TD2+
6	TD2-
7	TD1-
8	TD3+
9	TD3-
10	GND

Table 3-3   USB Connector (J6)

NOTE: J6 is assembled only on ENP1	
Pin Number	**Signal Description**
1	+5V
2	Data -
3	Data +
4	GND

3.3.1.2   Backplane Connectors

Table 3-4   P1 Connectors and Signal Descriptions

P1 Connector (1st Row)		**P1 Connector (2nd Row)**		**P1 Connector (3rd Row)**		**P1 Connector (4th Row)**		**P1 Connector (5th Row)**	
Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Desc
A1	DATA 0	B1	BBSY	C1	DATA 8	D1	+5V	Z1	NC
A2	DATA 1	B2	BCLR	C2	DATA 9	D2	GND	Z2	GND
A3	DATA 2	B3	ACFAIL	C3	DATA 10	D3	NC	Z3	NC

Table 3-4   P1 Connectors and Signal Descriptions (continued)

P1 Connector (1st Row)		P1 Connector (2nd Row)		P1 Connector (3rd Row)		P1 Connector (4th Row)		P1 Connector (5th Row)	
Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Desc
A4	DATA 3	B4	BGIN0	C4	DATA 11	D4	NC	Z4	GND
A5	DATA 4	B5	BGOUT0	C5	DATA 12	D5	NC	Z5	NC
A6	DATA 5	B6	BGIN1	C6	DATA 13	D6	NC	Z6	GND
A7	DATA 6	B7	BGOUT1	C7	DATA 14	D7	NC	Z7	NC
A8	DATA 7	B8	BGIN2	C8	DATA 15	D8	NC	Z8	GND
A9	GND	B9	BGOUT2	C9	GND	D9	GAP	Z9	NC
A10	SYSCLK	B10	BGIN3	C10	SYSFAIL	D10	GA0	Z10	GND
A11	GND	B11	BGOUT3	C11	BERR	D11	GA1	Z11	NC
A12	DS1	B12	BR0	C12	SYSRESET	D12	+3.3V (not used)	Z12	GND
A13	DS0	B13	BR1	C13	LWORD	D13	GA2	Z13	NC
A14	WRITE	B14	BR2	C14	AM 5	D14	+3.3V (not used)	Z14	GND
A15	GND	B15	BR3	C15	ADD 23	D15	GA3	Z15	NC
A16	DTACK	B16	AM 0	C16	ADD 22	D16	+3.3V (not used)	Z16	GND
A17	GND	B17	AM 1	C17	ADD 21	D17	GA4	Z17	NC
A18	AS	B18	AM 2	C18	ADD 20	D18	+3.3V (not used)	Z18	GND
A19	GND	B19	AM 3	C19	ADD 19	D19	NC	Z19	NC
A20	IACK	B20	GND	C20	ADD 18	D20	+3.3V (not used)	Z20	GND
A21	IACKIN	B21	NC	C21	ADD 17	D21	NC	Z21	NC

Table 3-4   P1 Connectors and Signal Descriptions (continued)

P1 Connector (1st Row)		P1 Connector (2nd Row)		P1 Connector (3rd Row)		P1 Connector (4th Row)		P1 Connector (5th Row)	
Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Desc
A22	IACKOUT	B22	NC	C22	ADD 16	D22	+3.3V (not used)	Z22	GND
A23	AM 4	B23	GND	C23	ADD 15	D23	NC	Z23	NC
A24	ADD 7	B24	IRQ7	C24	ADD 14	D24	+3.3V (not used)	Z24	GND
A25	ADD 6	B25	IRQ6	C25	ADD 13	D25	NC	Z25	NC
A26	ADD 5	B26	IRQ5	C26	ADD 12	D26	+3.3V (not used)	Z26	GND
A27	ADD 4	B27	IRQ4	C27	ADD 11	D27	NC	Z27	NC
A28	ADD 3	B28	IRQ3	C28	ADD 10	D28	+3.3V (not used)	Z28	GND
A29	ADD 2	B29	IRQ2	C29	ADD 9	D29	NC	Z29	NC
A30	ADD 1	B30	IRQ1	C30	ADD 8	D30	+3.3V (not used)	Z30	GND
A31	-12V	B31	+5V_STDBY	C31	+12V	D31	GND	Z31	NC
A32	+5V	B32	+5V	C32	+5V	D32	+5V	Z32	GND

Table 3-5   P2 Connectors and Signal Descriptions

P2 Connector (1st Row)		P2 Connector (2nd Row)		P2 Connector (3rd Row)		P2 Connector (4th Row)		P2 Connector (5th Row)	
Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Desc.
A1	PMC IO 2	B1	+5V	C1	PMC IO 1	D1	NC	Z1	GIGE3_ MDIO0_ P
A2	PMC IO 4	B2	GND	C2	PMC IO 3	D2	NC	Z2	GND

Table 3-5   P2 Connectors and Signal Descriptions (continued)

P2 Connector (1st Row)		P2 Connector (2nd Row)		P2 Connector (3rd Row		P2 Connector (4th Row)		P2 Connector (5th Row)	
Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Desc.
A3	PMC IO 6	B3	RETRY	C3	PMC IO 5	D3	GND	Z3	GIGE3_MDIO0_N
A4	PMC IO 8	B4	ADDRESS 24	C4	PMC IO 7	D4	USB1_P	Z4	GND
A5	PMC IO 10	B5	ADDRESS 25	C5	PMC IO 9	D5	USB1_N	Z5	GIGE3_MDIO1_P
A6	PMC IO 12	B6	ADDRESS 26	C6	PMC IO 11	D6	GND	Z6	GND
A7	PMC IO 14	B7	ADDRESS 27	C7	PMC IO 13	D7	USB2_P	Z7	GIGE3_MDIO1_N
A8	PMC IO 16	B8	ADDRESS 28	C8	PMC IO 15	D8	USB2_N	Z8	GND
A9	PMC IO 18	B9	ADDRESS 29	C9	PMC IO 17	D9	RTM_SIO	Z9	GIGE3_MDIO2_P
A10	PMC IO 20	B10	ADDRESS 30	C10	PMC IO 19	D10	BPSWITCH_N	Z10	GND
A11	PMC IO 22	B11	ADDRESS 31	C11	PMC IO 21	D11	GPIO_2	Z11	GIGE3_MDIO2_N
A12	PMC IO 24	B12	GND	C12	PMC IO 23	D12	GPIO_3	Z12	GND
A13	PMC IO 26	B13	+5V	C13	PMC IO 25	D13	I2C DATA	Z13	GIGE3_MDIO3_P
A14	PMC IO 28	B14	DATA 16	C14	PMC IO 27	D14	I2C CLK	Z14	GND

Table 3-5   P2 Connectors and Signal Descriptions (continued)

P2 Connector (1st Row)		P2 Connector (2nd Row)		P2 Connector (3rd Row		P2 Connector (4th Row)		P2 Connector (5th Row)	
Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Desc.
A15	PMC IO 30	B15	DATA 17	C15	PMC IO 29	D15	COM1_RX /COM1_R X_N	Z15	GIGE3_ MDIO3_ N
A16	PMC IO 32	B16	DATA 18	C16	PMC IO 31	D16	COM1_CT S_N/COM 1_RX_P	Z16	GND
A17	PMC IO 34	B17	DATA 19	C17	PMC IO 33	D17	COM2_RX /COM2_R X_N	Z17	GIGE4_ MDIO0_ P
A18	PMC IO 36	B18	DATA 20	C18	PMC IO 35	D18	COM2_CT S_N/COM 2_RX_P	Z18	GND
A19	PMC IO 38	B19	DATA 21	C19	PMC IO 37	D19	COM3_RX /COM3_R X_N	Z19	GIGE4_ MDIO0_ N
A20	PMC IO 40	B20	DATA 22	C20	PMC IO 39	D20	COM3_CT S_N/COM 3_RX_P	Z20	GND
A21	PMC IO 42	B21	DATA 23	C21	PMC IO 41	D21	COM4_RX /COM4_R X_N	Z21	GIGE4_ MDIO1_ P
A22	PMC IO 44	B22	GND	C22	PMC IO 43	D22	COM4_CT S_N/COM 4_RX_P	Z22	GND
A23	PMC IO 46	B23	DATA 24	C23	PMC IO 45	D23	COM1_TX /COM1_T X_N	Z23	GIGE4_ MDIO1_ N
A24	PMC IO 48	B24	DATA 25	C24	PMC IO 47	D24	COM1_RT S_N/COM 1_TX_P	Z24	GND

Table 3-5   P2 Connectors and Signal Descriptions (continued)

P2 Connector (1st Row)		P2 Connector (2nd Row)		P2 Connector (3rd Row		P2 Connector (4th Row)		P2 Connector (5th Row)	
Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Description	Pin Name	Signal Desc.
A25	PMC IO 50	B25	DATA 26	C25	PMC IO 49	D25	COM2_TX /COM2_TX_N	Z25	GIGE4_ MDIO2_ P
A26	PMC IO 52	B26	DATA 27	C26	PMC IO 51	D26	COM2_RTS_N/COM2_TX_P	Z26	GND
A27	PMC IO 54	B27	DATA 28	C27	PMC IO 53	D27	COM3_TX /COM3_TX_N	Z27	GIGE4_ MDIO2_ N
A28	PMC IO 56	B28	DATA 29	C28	PMC IO 55	D28	COM3_RTS_N/COM3_TX_P	Z28	GND
A29	PMC IO 58	B29	DATA 30	C29	PMC IO 57	D29	COM4_TX /COM4_TX_N	Z29	GIGE4_ MDIO3_ P
A30	PMC IO 60	B30	DATA 31	C30	PMC IO 59	D30	COM4_RTS_N/COM4_TX_P	Z30	GND
A31	PMC IO 62	B31	GND	C31	PMC IO 61	D31	GND	Z31	GIGE4_ MDIO3_ N
A32	PMC IO 64	B32	+5V	C32	PMC IO 63	D32	+5V	Z32	GND

Table 3-6   VXS P0 Connector (applicable to MVME8100 only)

Pin	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	NC	GND	P1_TX0_N	P1_TX0_P	GND	P1_RX0_N	P1_RX0_P
2	GND	P1_TX1_N	P1_TX1_P	GND	P1_RX1_N	P1_RX1_P	GND
3	NC	GND	P1_TX2_N	P1_TX2_P	GND	P1_RX2_N	P1_RX2_P
4	GND	P1_TX3_N	P1_TX3_P	GND	P1_RX3_N	P1_RX3_P	GND

Table 3-6   VXS P0 Connector (applicable to MVME8100 only) (continued)

Pin	Row G	Row F	Row E	Row D	Row C	Row B	Row A
5	NC	GND	SG_TX0_N	SG_TX0_P	GND	SG_RX0_N	SG_RX0_P
6	GND	NC	NC	GND	NC	NC	GND
7	GPIO0	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	GPIO1	GND	NC	NC	GND	NC	NC
10	GND	SATA_TX_N	SATA_TX_P	GND	SATA_RX_N	SATA_RX_P	GND
11	NC	GND	SG_TX1_N	SG_TX1_P	GND	SG_RX1_N	SG_RX1_P
12	GND	P2_TX0_N	P2_TX0_P	GND	P2_RX0_N	P2_RX0_P	GND
13	NC	GND	P2_TX1_N	P2_TX1_P	GND	P2_RX1_N	P2_RX1_P
14	GND	P2_TX2_N	P2_TX2_P	GND	P2_RX2_N	P2_RX2_P	GND
15	NC	GND	P2_TX3_N	P2_TX3_P	GND	P2_RX3_N	P2_RX3_P

3.3.2   On-Board Connectors

The on-board customized SATA connector is compatible with the MVME8100 SATA kit.

Following are the on-board connectors:

- SATA connector
- PMC connector
- Asset Joint Test Access Group (JTAG) connector
- Common On-chip Processor (COP) connector
- XMC connector

SATA Connector

The on-board customized SATA connector is compatible with the Penguin Solutions SATA kit MVME8100-HDMTKIT4.

Table 3-7   Customized SATA Connector (J3)

Pin Name	Signal Description	Pin Name	Signal Description
1	GND	21	GND
2	GND	22	SATA POWER ENABLE
3	NC	23	NC
4	SATA TX +	24	SATA DETECT
5	NC	25	NC
6	SATA TX -	26	GND
7	GND	27	GND
8	GND	28	GND
9	GND	29	GND
10	GND	30	GND
11	NC	31	+3.3V
12	SATA RX -	32	+5V
13	NC	33	+3.3V
14	SATA RX +	34	+5V
15	GND	35	+3.3V
16	GND	36	+5V
17	NC	37	+3.3V
18	GND	38	+5V
19	NC	39	+3.3V
20	GND	40	+5V

PMC Connectors

The MVME8100 Series boards support two PMC sites. The connector is located on the middle portion of the board. It uses J14 to support PMC I/O that goes to RTM PMC.

Table 3-8   PMC J11/J21 Connector and Signal Description

Pin Name	Signal Description	Pin Name	Signal Description
1	JTAG TCK	33	FRAME
2	-12V	34	GND
3	GND	35	GND
4	INT A	36	IRDY
5	INT B	37	DEVSEL
6	INT C	38	+5V
7	PRESENT SIGNAL	39	PCIXCAP
8	+5V	40	LOCK
9	INT D	41	NC
10	NC	42	NC
11	GND	43	PAR
12	3.3 V AUX	44	GND
13	PCI CLK	45	+3.3V
14	GND	46	AD 15
15	GND	47	AD 12
16	GNT A	48	AD 11
17	REQ A	49	AD 9
18	+5V	50	+5V
19	+3.3V	51	GND
20	AD 31	52	CBE0
21	AD 28	53	AD 6

Table 3-8   PMC J11/J21 Connector and Signal Description (continued)

Pin Name	Signal Description	Pin Name	Signal Description
22	AD 27	54	AD 5
23	AD 25	55	AD 4
24	GND	56	GND
25	GND	57	+3.3V
26	CBE3	58	AD 3
27	AD 22	59	AD 2
28	AD 21	60	AD 1
29	AD 19	61	AD 0
30	+5V	62	+5V
31	+3.3V	63	GND
32	AD 17	64	REQ64

Table 3-9   PMC J12/J22 Connector and Signal Descriptions

Pin Name	Signal Description	Pin Name	Signal Description
1	+12V	33	GND
2	JTAG TRST	34	IDSELB
3	JTAG TMS	35	TRDY
4	JTAG TDO	36	+3.3V
5	JTAG TDI	37	GND
6	GND	38	STOP
7	GND	39	PERR
8	NC	40	GND
9	NC	41	+3.3V
10	NC	42	SERR
11	BUSMODE2 (Pulled UP)	43	CBE1

Table 3-9   PMC J12/J22 Connector and Signal Descriptions (continued)

Pin Name	Signal Description	Pin Name	Signal Description
12	+3.3V	44	GND
13	PCI RESET	45	AD 14
14	BUSMODE3 (PULLED DWN)	46	AD 13
15	+3.3V	47	M66EN
16	BUSMODE4 (PULLED DWN)	48	AD 10
17	NC	49	AD 8
18	GND	50	+3.3V
19	AD 30	51	AD 7
20	AD 29	52	REQB
21	GND	53	+3.3V
22	AD 26	54	GNTB
23	AD 24	55	NC
24	+3.3V	56	GND
25	IDSEL	57	NC
26	AD 23	58	EREADY
27	+3.3V	59	GND
28	AD 20	60	RSTOUT
29	AD 18	61	ACK64
30	GND	62	+3.3V
31	AD 16	63	GND
32	CBE2	64	NC

Table 3-10   PMC J13/J23 Connectors and Signal Descriptions

Pin Name	Signal Description	Pin Name	Signal Description
1	NC	33	GND
2	GND	34	AD48
3	GND	35	AD 47
4	CBE7	36	AD 46
5	CBE6	37	AD 45
6	CBE5	38	GND
7	CBE4	39	+3.3V
8	GND	40	AD 44
9	+3.3V	41	AD 43
10	PAR64	42	AD 42
11	AD 63	43	AD 41
12	AD 62	44	GND
13	AD 61	45	GND
14	GND	46	AD 40
15	GND	47	AD 39
16	AD 60	48	AD 38
17	AD 59	49	AD 37
18	AD 58	50	GND
19	AD 57	51	GND
20	GND	52	AD 36
21	+3.3V	53	AD 35
22	AD 56	54	AD 34

Table 3-10   PMC J13/J23 Connectors and Signal Descriptions (continued)

Pin Name	Signal Description	Pin Name	Signal Description
23	AD 55	55	AD 33
24	AD 54	56	GND
25	AD 53	57	+3.3V
26	GND	58	AD 32
27	GND	59	NC
28	AD 52	60	NC
29	AD 51	61	NC
30	AD 50	62	GND
31	AD 49	63	GND
32	GND	64	NC

Table 3-11   PMC J14 Connectors and Signal Descriptions

Pin Name	Signal Description	Pin Name	Signal Description
1	PMC IO 1	33	PMC IO 33
2	PMC IO 2	34	PMC IO 34
3	PMC IO 3	35	PMC IO 35
4	PMC IO 4	36	PMC IO 36
5	PMC IO 5	37	PMC IO 37
6	PMC IO 6	38	PMC IO 38
7	PMC IO 7	39	PMC IO 39
8	PMC IO 8	40	PMC IO 40
9	PMC IO 9	41	PMC IO 41
10	PMC IO 10	42	PMC IO 42
11	PMC IO 11	43	PMC IO 43

Table 3-11   PMC J14 Connectors and Signal Descriptions (continued)

Pin Name	Signal Description	Pin Name	Signal Description
12	PMC IO 12	44	PMC IO 44
13	PMC IO 13	45	PMC IO 45
14	PMC IO 14	46	PMC IO 46
15	PMC IO 15	47	PMC IO 47
16	PMC IO 16	48	PMC IO 48
17	PMC IO 17	49	PMC IO 49
18	PMC IO 18	50	PMC IO 50
19	PMC IO 19	51	PMC IO 51
20	PMC IO 20	52	PMC IO 52
21	PMC IO 21	53	PMC IO 53
22	PMC IO 22	54	PMC IO 54
23	PMC IO 23	55	PMC IO 55
24	PMC IO 24	56	PMC IO 56
25	PMC IO 25	57	PMC IO 57
26	PMC IO 26	58	PMC IO 58
27	PMC IO 27	59	PMC IO 59
28	PMC IO 28	60	PMC IO 60
29	PMC IO 29	61	PMC IO 61
30	PMC IO 30	62	PMC IO 62
31	PMC IO 31	63	PMC IO 63
32	PMC IO 32	64	PMC IO 64

Asset JTAG Connector

The MVME8100 Series boards contain a 20-pin 0.1" header for an Asset JTAG header. The pinout for the header is given in the following table.

Table 3-12   Asset JTAG Header Pin Assignment (P12)

Pin Number	Description	Pin Number	Description
1	TCK	2	ASSET_PRSNT_L (GND on cable)
3	TDO	4	GND
5	TMS	6	GND
7	TRST_L	8	GND
9	TDI	10	GND
11	No Pin Key	12	Reserved - NC
13	GND	14	Reserved - NC
15	GND	16	Reserved - NC
17	GND	18	Reserved - NC
19	GND	20	Reserved - NC

XMC Connector

MVME8100 Series boards support two XMC sites. The board only supports J15 for XMC site 1 and J25 for XMC site 2.

Table 3-13   XMC Connectors and Signal Descriptions

XJ1/2 (Row A)		XJ1/2 (Row B)		XJ1/2 (Row C)		XJ1/2 (Row D)		XJ1/2 (Row E)		XJ1/2 (Row F)	
Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.
1	RX0 +	1	RX0 -	1	+3.3V	1	RX1 +	1	RX1 -	1	+3.3V
2	GND	2	GND	2	JTAG TRST	2	GND	2	GND	2	HRESET
Note1: All * are NC on XJ2											
Note2: Default configuration: XMC1 is x8; XMC2 is x4											

Table 3-13   XMC Connectors and Signal Descriptions (continued)

XJ1/2 (Row A)		XJ1/2 (Row B)		XJ1/2 (Row C)		XJ1/2 (Row D)		XJ1/2 (Row E)		XJ1/2 (Row F)	
Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.
3	RX2 +	3	RX2 -	3	+3.3V	3	RX3 +	3	RX3 -	3	+3.3V
4	GND	4	GND	4	JTAG TCK	4	GND	4	GND	4	MRSTO (PULLED UP)
5	RX4 + *	5	RX4 - *	5	+3.3V	5	RX5 + *	5	RX5 - *	5	+3.3V
6	GND	6	GND	6	JTAG TMS	6	GND	6	GND	6	+12V
7	RX6 + *	7	RX6 - *	7	+3.3V	7	RX7 + *	7	RX7 - *	7	+3.3V
8	GND	8	GND	8	JTAG TDI	8	GND	8	GND	8	-12V
9	NC	9	NC	9	NC	9	NC	9	NC	9	+3.3V
10	GND	10	GND	10	JTAG TDO	10	GND	10	GND	10	GA 0
11	TX0 +	11	TX0 -	11	BIST (PULLED UP)	11	TX1 +	11	TX1 -	11	+3.3V
12	GND	12	GND	12	GA 1	12	GND	12	GND	12	PRESENT
13	TX2 +	13	TX2 -	13	3.3V AUX	13	TX3 +	13	TX3 -	13	+3.3V
14	GND	14	GND	14	GA 2	14	GND	14	GND	14	I2C DATA
15	TX4 + *	15	TX4 - *	15	NC	15	TX5 + *	15	TX5 - *	15	+3.3V
16	GND	16	GND	16	MVMRO (PULLED DOWN)	16	GND	16	GND	16	I2C CLOCK
17	TX6 + *	17	TX6 - *	17	NC	17	TX7 + *	17	TX7 - *	17	NC
Note1: All * are NC on XJ2											
Note2: Default configuration: XMC1 is x8; XMC2 is x4											

Table 3-13   XMC Connectors and Signal Descriptions (continued)

XJ1/2 (Row A)		XJ1/2 (Row B)		XJ1/2 (Row C)		XJ1/2 (Row D)		XJ1/2 (Row E)		XJ1/2 (Row F)	
Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.	Pin No	Signal Desc.
18	GND	18	GND	18	NC	18	GND	18	GND	18	NC
19	CLK +	19	CLK -	19	NC	19	NC	19	ROOT0 (PULLED UP)	19	NC

Note1: All * are NC on XJ2

Note2: Default configuration: XMC1 is x8; XMC2 is x4

3.4   LEDS

The next table describes the LEDs on the front panel of the MVME8100 Series boards. Refer to *Figure 3-1* for LED locations.

Table 3-14   Front Panel LEDs

Label	Function	Color	Description
USER 1 (D16)	User Defined	Off	By Default
		Yellow	User Software Controllable.
		Red	User Software Controllable.
FAIL (D8)	Board Fail	Off	Normal operation after successful firmware boot
		Red	One or more on-board power rails have failed and the board has shutdown to protect the hardware. Normal during power up, during hardware reset (such as a front panel reset). May be asserted by the BDFAIL bit in the Tsi148 VSTAT register
SPEED (J4)	Link/Speed	Off	No link
		Amber	10/100BASE-T operation
		Green	1000 BASE-T operation

Table 3-14   Front Panel LEDs (continued)

Label	Function	Color	Description
ACT (J4)	Activity	Off	No activity
		Blinking Green	Activity proportional to bandwidth utilization

3.4.1   On-board LEDs

The on-board LEDs are listed below. The LEDs are located on the rear side of the board just opposite of the battery location. To view the board, see *Figure 3-1 on page 51*.

Table 3-15   On-board LEDs Status

Label	Function	Color	Description
D32	MMC Write Protect	off	WP disabled
		Green	WP enabled
D33	ENP1: PS1_LED_N		
	ENP4: Board FAIL	Amber	
D34	ENP1: PS2_LED_N		
	ENP4: POWER	Green	
D35	ENP1: PS3_LED_N		
	ENP4: RESET	Amber	
D19	USR_LED2_N	Red	
	USR_LED3_N	Yellow	

3.5   Switches

The board provides the following configuration switches:

- S2 switch
- S3 switch
- S4 switch
- S5 switch

- Reset/Abort switch

3.5.1   Configuration Switches

The following sections describe the on-board switches and their configurations.

	Board Malfunction
⚠️	**Switches marked as Reserved might carry production-related functions and can cause the board to malfunction if their setting is changed.**
	Do not change settings of switches marked as Reserved. The setting of switches which are not marked as Reserved has to be checked and changed before board installation.

3.5.1.1   S2 Switch

The Switch Bank S2 provides watchdog control, serial port configuration and P0 fabric selection.

Table 3-16   S2 Switch Settings

Position	Default	Description
1	OFF	OFF - Watchdog Disabled ON - Watchdog Enabled
2	OFF	OFF - Serial Console Port to Front Panel ON - Serial Console Port to P2/RTM panel
3	OFF	OFF - P2 Serial Port 0 is RS-232 ON - P2 Serial Port 0 is RS-422/485
4	OFF	OFF - P2 Serial Port 1 is RS-232 ON - P2 Serial Port 1 is RS-422/485
5	OFF	OFF - P2 Serial Port 2 is RS-232 ON - P2 Serial Port 2 is RS-422/485
6	OFF	OFF - P2 Serial Port 3 is RS-232 ON - P2 Serial Port 3 is RS-422/485
7	OFF	OFF - Front Panel console Port is RS-232 ON - Front Panel console Port is RS-422/485
8	OFF	OFF - Select SRIO for P0 Backplane Fabric (applicable to MVME8100 only) ON - Select PCIe for P0 Backplane Fabric (applicable to MVME8100 only)

3.5.1.2 S3 Switch

The TSI148 VMEbus Status Register provides the VMEbus geographical address of the MVME8100 Series boards. Applications not using a 5-row backplane can use these switches to manually assign board's VMEbus geographical address. Note that this switch is wired parallel with geographical address pins on the 5-row connector to these switches must be in the off position when installed in a 5-row chassis in order to get the correct address from P1 connector. This switch reflects the inverted states on the geographical address signals.

Table 3-17   S3 Switch Settings

Position	Default	Description
1	OFF	OFF - SPI FLASH Write Protect is Disabled ON - SPI FLASH Write Protect is Enabled
2	OFF	P0 Connector Port B PCIE/SRIO Fabric Selection (Applicable to MVME8100 only) OFF- Port B same as Port A selection and is controlled by SW2-8 ON - Port B selection is opposite Port A and is controlled by S2-8 selection
3	OFF (1)	GAP#
4	OFF (1)	GA4#
5	OFF (1)	GA3#
6	OFF (1)	GA2#
7	OFF (1)	GA1#
8	OFF (1)	GA0#

Below is the switch configuration for corresponding slot address in a 21 slot chassis 3-row backplane.

Table 3-18   Three Row Backplane Manual Slot Addressing

S1-3	S1-4	S1-5	S1-6	S1-7	S1-8	GAP# GA(4:0)#	Slot Address
OFF	OFF	OFF	OFF	OFF	ON	1 11110	1
OFF	OFF	OFF	OFF	ON	OFF	1 11101	2
ON	OFF	OFF	OFF	ON	ON	0 11100	3
OFF	OFF	OFF	ON	OFF	OFF	1 11011	4

Table 3-18   Three Row Backplane Manual Slot Addressing (continued)

S1-3	S1-4	S1-5	S1-6	S1-7	S1-8	GAP# GA(4:0)#	Slot Address
ON	OFF	OFF	ON	OFF	ON	0 11010	5
ON	OFF	OFF	ON	ON	OFF	0 11001	6
OFF	OFF	OFF	ON	ON	ON	1 11000	7
OFF	OFF	ON	OFF	OFF	OFF	1 10111	8
ON	OFF	ON	OFF	OFF	ON	0 10110	9
ON	OFF	ON	OFF	ON	OFF	0 10101	10
OFF	OFF	ON	OFF	ON	ON	1 10100	11
ON	OFF	ON	ON	OFF	OFF	0 10011	12
OFF	OFF	ON	ON	OFF	ON	1 10010	13
OFF	OFF	ON	ON	ON	OFF	1 10001	14
ON	OFF	ON	ON	ON	ON	0 10000	15
OFF	ON	OFF	OFF	OFF	OFF	1 01111	16
ON	ON	OFF	OFF	OFF	ON	0 01110	17
ON	ON	OFF	OFF	ON	OFF	0 01100	18
OFF	ON	OFF	OFF	ON	ON	1 01100	19
ON	ON	OFF	ON	OFF	OFF	0 01011	20
OFF	ON	OFF	ON	OFF	ON	1 01010	21

3.5.1.3 S4 Switch

The S4 switch includes the SCON control and PCIE/SRIO P0 root complex/endpoint configuration switches for MVME8100. The S4 switch of MVME8105/MVME8110 includes SCON control only. The VME SCON AUTO switch is OFF to select Auto-SCON mode. The switch is ON to select manual SCON mode which works in conjunction with the VME SCON SEL switch. The VME_SCON_SEL switch is OFF to manually select SCON mode. This switch is ON to manually select non-SYSCON mode. This switch is only effective when the VME SCON AUTO switch is ON.

Table 3-19   S4 Switch Settings

Position	Default	Description
1	OFF	Clear Environment Variables OFF - Disable Clear Environment Variables ON - Enable Clear Environment Variables. At reset, U-Boot ENV variables are set to default values.
2	OFF	OFF - Configure PCIe/SRIo Switches as P0 Root Complex (applicable to MVME8100 only) ON - Configure PCIe/SRIO Switches as P0 Endpoint (applicable to MVME8100 only)
3	OFF	OFF - Auto VME System Controller ON - Manual VME System Controller
4	OFF	OFF - VME System Controller ON - VME Non-System Controller

3.5.1.4 S5 Switch

The switch Bank S5 provides the boot SPI FLASH selection.

Table 3-20   S5 Switch Settings

Position	Default	Description
1	OFF	OFF - Boot from SPI FLASH 0 ON - Boot from SPI FLASH 1
2	OFF	Reserved

3.5.1.5   Reset /Abort Switch

A dual function switch is located on the front panel. This switch can function either as a Reset or Abort button. If the button is pressed for less than 3 seconds, the CPLD generates an abort interrupt to the P5020 / P5010 processor. If the button is pressed for more than 3 seconds, the CPLD generates a board hard reset. If the board is configured as System Controller, the backplane VME SYSRESET signal is also asserted during a board hard reset.

Functional Description

4.1   Overview

The MVME8100 single board computer is a 6U VME/VXS board based on the NXP QorIQ P5020 processor. The MVME8105 single board computer is a 6U VME board based on the NXP QorIQ P5020 processor. The MVME8110 single board computer is a 6U VME board based on the NXP QorIQ P5010 processor.

This section describes the features of the MVME8100 Series boards.

4.2   Block Diagrams

The following figures show the block diagrams of the MVME8100, MVME8105 and MVME8110 architecture.

Figure 4-1   Block Diagram of MVME8100
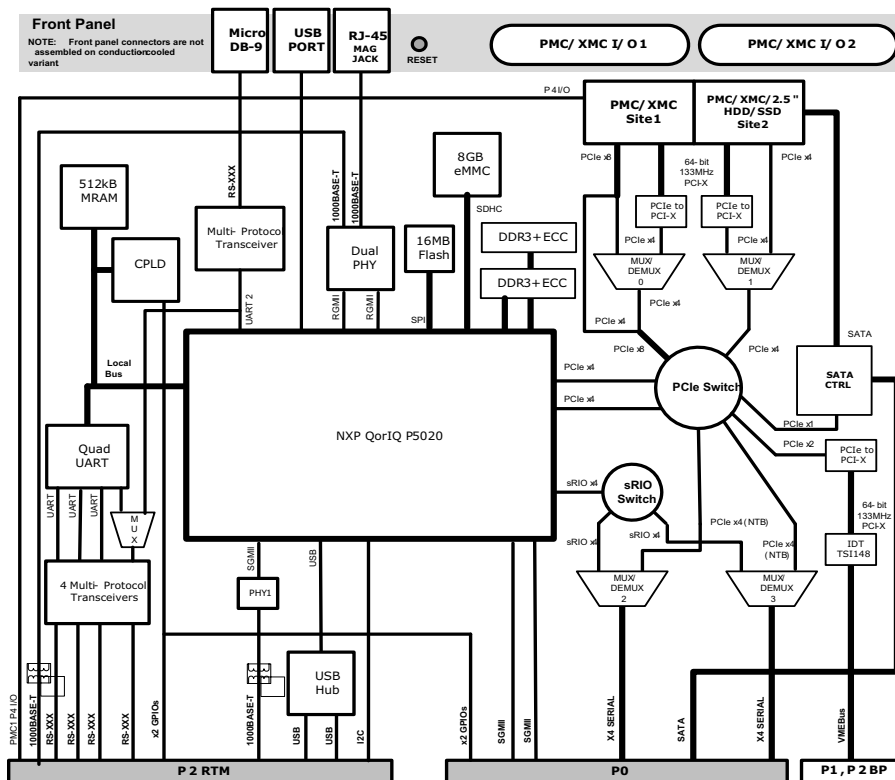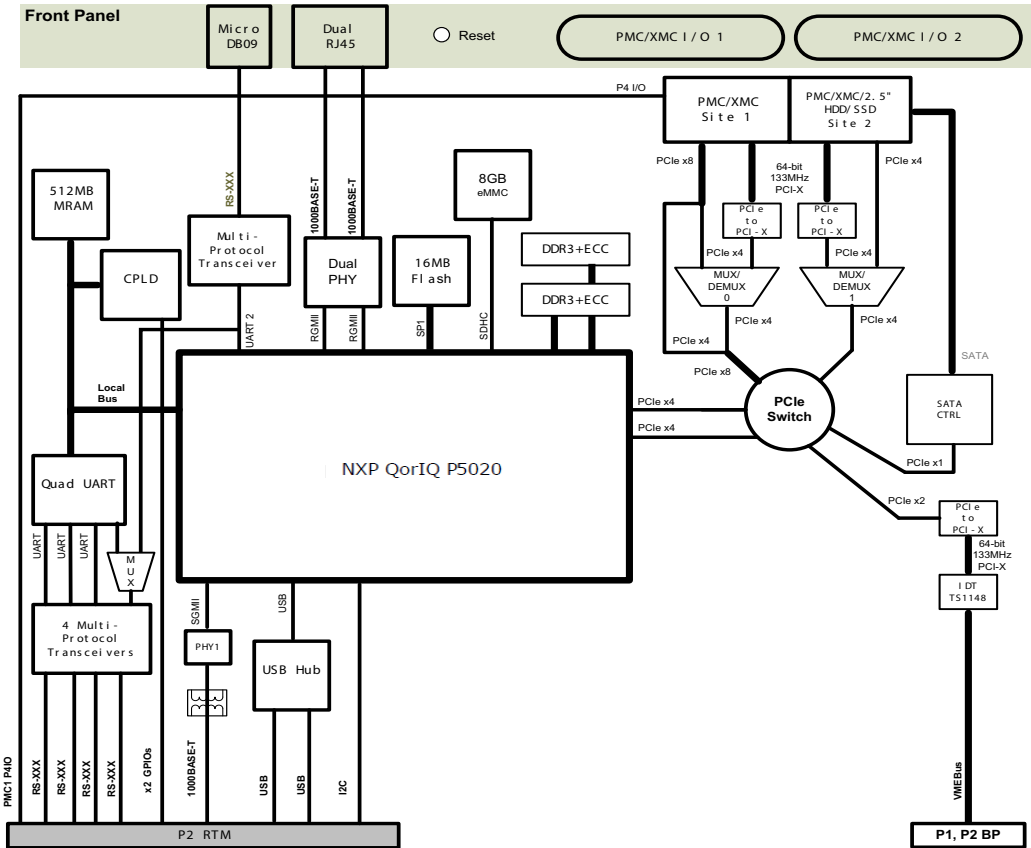
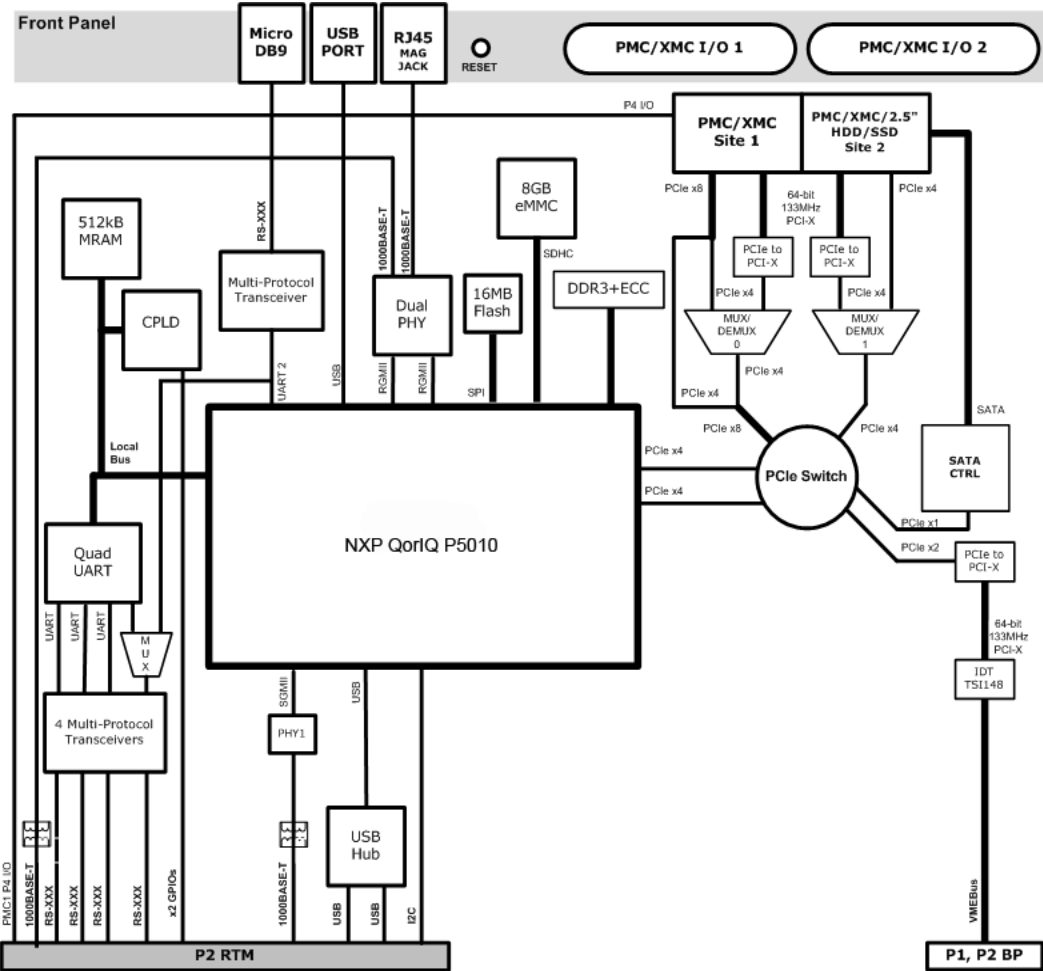## Figure 4-2   Block Diagram of MVME8105

Figure 4-3   Block Diagram of MVME8110

4.3   Processor

The P5020 QorIQ processor combines two Power Architecture processor cores with high-performance data path acceleration logic and network. The processor also features peripheral bus interfaces for networking, telecom/datacom, wireless infrastructure, and aerospace applications.

The P5010 QorIQ processor has only one Power Architecture processor core.

This device can be used for combined control, data path and application layer processing in routers, switches, base station controllers, and general-purpose embedded computing. Its high level of integration offers significant performance benefits compared to multiple discrete devices while also greatly simplifies the board design.

The MVME8100/MVME8105 board ENP1 version is designed to use the 2.0GHz core processor version while the ENP4 version uses the 1.8GHz processor. The MVME8110 board ENP1 version is designed to use the 1.2GHz core processor.

The MVME8105 only has the 2.0GHz version and does not have the ENP4 version. For more information, refer to the NXP QorIQ P5020/P5010 Integrated Multicore Communications Processor Family Reference Manual.

4.4   System Memory

The MVME8100/MVME8105 supports four GB DDR3 ECC memory using two banks of 2Gb memory devices. The MVME8110 supports memory using one bank of 2Gb memory devices.

The memory devices are soldered-down and not modular solution using Dual In-line Memory Module (DIMM) sockets. The supported data rate is 1333MT/s. The memory is evenly-distributed across both memory channels (e.g., memory-capacity requirement is 4GB, place 2GB of memory on each channel).

4.5 Timers

This section describes the timer functions implemented on the boards.

4.5.1 Real Time Clock

The MVME8100 implements an Real Time Clock (RTC) to maintain seconds, minutes, hours, day, date, month, and year accurately. It includes a 32.768KHz crystal, DS1337 RTC, and back-up power.   For the ENP1 versions of the boards, a battery is used for the RTC back-up power. For the ENP4 version, a 3.3V regulator powered from the VME backplane +5V_STDBY voltage is used for back-up power. The DS1337 has an interrupt output (INTA) which can be programmed to assert a processor IRQ on a time/day/date match.   The DS1337 also has a 32.768KHz clock output (SQW) which is used to drive the P5020/P5010 RTC input signal.

The RTC internal oscillator was disabled before the board was shipped from the factory. Use the following process to turn on the RTC oscillator from U-Boot:

```
MVME8100 => i2c mm 0x68 e.1
0000000e: 98 ? 18
0000000f: 80 ? n
```

To set the date, use the following U-Boot command:

```
MVME8100 =>date [MMDDhhmm[[CC]YY][.ss]]
```

4.5.2 P5020/P5010 Internal Timers

The P5020/P5010 provides a total of eight global timers and is divided into two groups, group A and group B. Each group has four timers. Each timer has four individual configuration register. However, these two groups of timers cannot be cascaded together.

4.5.3 Watchdog Timers

The CPLD has two watchdogs timers, the Initial Hardware Watchdog (IWD) and the OS Watchdog (OSWD).

The Initial Hardware Watchdog is used to guard loading of U-Boot and to prevent board hanging up. U-Boot has to service IWD before timeout, or IWD will request Power-On Reset. Following a board reset, the board attempts to boot from the U-Boot flash selected by the configuration switches. If IWD is not serviced in time by U-Boot, then following the IWD reset, the board attempts to boot from the alternate SPI1 U-Boot flash device.

The OS Watchdog (OSWD) is used to guard loading of the operating system. The OS has to service OSWD before timeout or OSWD will request a hard reset sequence to reset the board.

If IWD is not serviced after switching over to the SPI1 U-Boot Flash, board will infinitely try to boot to SPI1 U-Boot Flash.

By default, U-Boot will disable both the IWD and the OSWD.

The configuration switch S2-1 is used to enable or disable both watchdogs. By default, the watchdogs are disabled.

4.5.3.1 Initial Hardware Watchdog

Initial Hardware Watchdog (IWD) starts after reset deassertion. This watchdog has to be serviced within 8s after a reset deassertion, otherwise a IWD reset will be requested.

The Initial Hardware Watchdog is serviced by writing 0xEEA1 to CPLD Command/Status Register.

4.5.3.2 OS Watchdog

The OS Watchdog (OSWD) is not armed after reset. It is enabled right after the IWD is disabled. The OSWD timeout is set to 108s. If the timer terminates, the OSWD reset sequence will be initiated.

OSWD is serviced and disabled by writing 0xBBC2 to CPLD Command/Status Register.

4.5.4 CPLD Tick Timer

The MVME8100 supports four independent 32-bit timers that are implemented on the CPLD to provide fully programmable registers for the timers.

4.6 Ethernet Interfaces

The P5020/P5010 has five dTSEC controllers. The controllers can be configured to implement RGMII, GMII, or SGMII interfaces to external Ethernet transceivers.

The MVME8100 Series boards use dTSEC4 for a dedicated front panel 10/100/1000BASE-T interface and dTSEC5 for a 10/100/1000BASE-T interface to the RTM via P2. MVME8105 uses dTSEC3 and dTSEC4 to the front panel. A Broadcom BCM5482 dual transceiver provides the RGMII -> 10/100/1000BASE-T interfaces. A second

10/100/1000BASE-T interface to the RTM through P2 is provided using dTSEC2 in SGMII mode. A Broadcom BCM54616S transceiver provides the SGMII -> 10/100/1000BASE-T interface. The registers of these transceivers can be accessed via the P5020 / P5010's two-wire Ethernet Management interface.

The front panel RJ-45 connector has integrated speed and activity status indicator LEDs. Similar to the front panel Ethernet, the RJ-45 connectors found in the RTM have integrated speed and activity status indicator LED's. Isolation transformers are provided on-board for each of the RTM ports.

The MVME8100 uses dTSEC1 and dTSEC5 in SGMII mode for two additional 1000Base-BX Ethernet ports to P0.

4.7 SPI Interface

Firmware boot Flash resides on the P5020/P5010 eSPI bus interface.

4.7.1 SPI Flash Memory

The P5020/P5010 contains two 8MB serial flash devices. These devices contain the 512 bits of the Reset Configuration Word, the boot firmware image (U-Boot), and the ENV environment variables.

4.7.2 Firmware Redundancy

The MVME8100 Series boards use two separate 8MB boot devices in order to provide boot firmware redundancy. The P5020 / P5010 SPI device controller uses Chip Select 0 as the boot device, so CPLD logic is used to swap the chip select to the boot devices. The chip select control is based upon the configuration switch S5-1.

At power-up, the selection of the SPI boot device is strictly based upon the switch S5-1 setting. The selected SPI device must contain a boot image. The MVME8100 Series boards support automatic SPI FLASH fail-over. If booting on one device is not successful, then the watchdog will trigger a board reset and the CPLD logic automatically toggle chip selects, and tries to boot on the other device.

4.8 MRAM

The MVME8100 Series boards include one MR2A16AVYS35/MR2A16AYS35 512KB MRAM device to provide a nonvolatile memory, that has virtually unlimited writes (100 trillion), fast access and ten years data retention without power. The MRAM is organized as 256Kx16 and accessible through the P5020/P5010 local bus.

4.9   eMMC

The MVME8100 Series boards contain a soldered down 8GB eMMC device connected to the P5020/P5010 eSDHC interface. The eSDHC interface operates in four bit MMC mode and supports up to 200Mbps data transfer for MMC card using four parallel data lines.

4.10   Processor Console Port

The MVME8100 Series boards use P5020 / P5010 UART1 port for the processor console interface. This console interface can be routed to the front panel or the P2 connector using configuration switches. The front panel port can be configured for RS-232 or RS-422/RS-485 modes. RS-232 mode supports RX, TX, RTS and CTS signals. Only four wire full duplex RX/TX is supported in RS-422/485 mode. The signaling mode is selected through on board configuration switches. The default baud rate on the front panel serial is 9600 baud.

The physical front panel console connector is a male micro-min DB-9. A male-to-male micro-mini DB-9 to DB-9 adapter cable is available under Penguin Solutions Part Number SERIAL MINI-D (30-W2400E01A).

4.11   Rear UART Ports

The MVME8100 Series boards provide four asynchronous serial UART interfaces to the P2 RTM connector by utilizing Exar's ST16C554 quad UART. The Quad Universal Asynchronous Receiver/Transmitter (QUART) features 16 bytes of transmit and receive First In First Out (FIFO), it has a selectable receive FIFO trigger levels and data rates of up to 1.5Mbps. Each UART has a set of registers that provide the user with operating status and control. The QUART is an 8-bit device connected to the P5020/P5010 through the local bus controller. QUART port A is multiplexed with the P5020/P5010 UART1 console port, so that the console port can be routed to the RTM COM1 port. The mux is controlled using configuration switches on S2.

The four ports can be configured for RS-232 or RS-422/RS-485 modes. RS-232 mode supports RX, TX, RTS and CTS signals. Only four wire full duplex RX/TX is supported in RS-422/485 mode. The signaling mode is selected through on board configuration switches on S2.

4.12 PCIe Ports

The MVME8100 Series boards provide multiple PCI Express ports. The P5020/P5010 is configured to use two x4 PCIe controllers (#1 and #3). Both controllers are configured to operate at Gen 1 data rate (2.5Gbaud). These ports are routed to an IDT 32NT24AG2 PCIe switch for expansion of the PCIe ports. The IDT switch is a 32-lane Gen 2 device and can support up to 24 ports, 8 of which are capable of NT function. Each port of the switch is configured to operate at Gen 1 data rate. The configuration of the ports and the partitioning of the switch into a single or multiple domains is controlled by an I^2C EEPROM connected to the PCIe switch master SMbus and loaded into the switch following reset.

The board provides two separate EEPROMs so that separate configuration data can be maintained for operating as a root complex or as an end point on the P0 connector ports for MVME8100. The selection of the root complex or end point EEPROM for loading the configuration data after reset is determined by the root complex configuration switch S4-2 (see *S4 Switch on page 76*.). The EEPROMs can be reprogrammed from the processor using the I^2C master interface in the IDT device. A swap bit in CPLD control register can be used to temporarily swap the EEPROM device addressing so that the alternate EEPROM can be reprogrammed. A diagram of the PCIe port configuration is shown in the following figure.

Figure 4-4 PCIe Ports
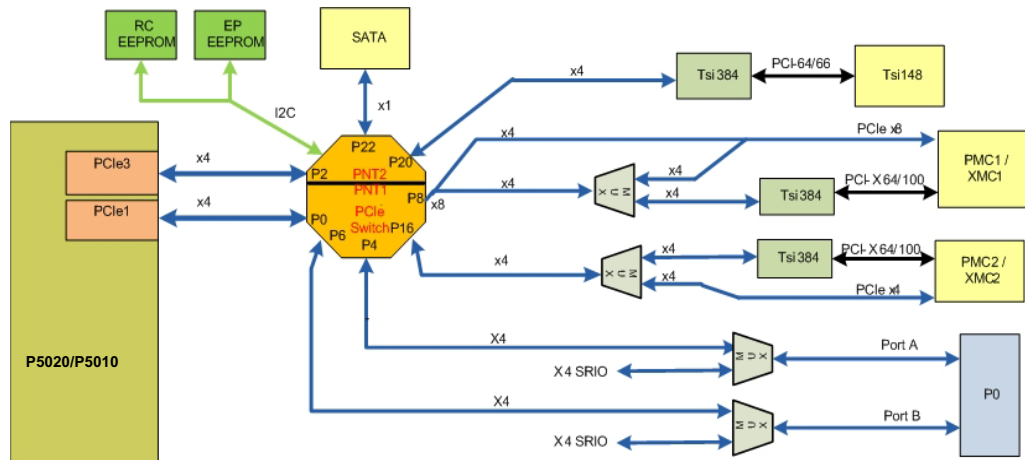
**NOTE:** P4 and P6 are disabled on MVME8105/MVME8110.

4.13   SRIO Ports

The MVME8100 also provides multiple SRIO ports. The P5020 provides a single x4 SRIO configured for 2.5GBaud data rate. This port is routed to an IDT 80HCPS1616 SRIO switch for expansion of the SRIO ports. The SRIO switch supports multiple lane speeds including 1.25, 2.5, 3.125 and 5.0Gbaud. The MVME8100 provides two x4 SRIO ports which may be routed to the P0 connector through a high speed mux. The selection of SRIO or PCIe ports to P0 is controlled by the S2-8 configuration switch (see *S2 Switch on page 73*). The configuration of the SRIO switch ports is controlled by an I^2C EEPROM connected to the SRIO switch I^2C bus and loaded into the switch following reset. The board provides two separate EEPROMs so that separate configuration data can be maintained for the MVME8100 operating as a root complex or as an end point on the P0 ports. The selection of the root complex or end point EEPROM for loading the configuration data after reset is determined by the root complex configuration switch S4-2 (see *S4 Switch on page 76*). The EEPROMs can be reprogrammed over the processor I^2C bus 4 interface. The EEPROM device addresses are listed in section *I2C Devices on page 91*.   A diagram of the SRIO port topology is shown in the following figure.

> **Important Information**
>
> **The 80HCPS1616 SRIO switch does not support auto baud rate discovery. The switch configuration EEPROMs must program the P0 fabric ports to match the SRIO baud rate of the system. The default baud rate for the P0 fabric ports is 2.5Gbaud.**

Figure 4-5   SRIO Bus Topology
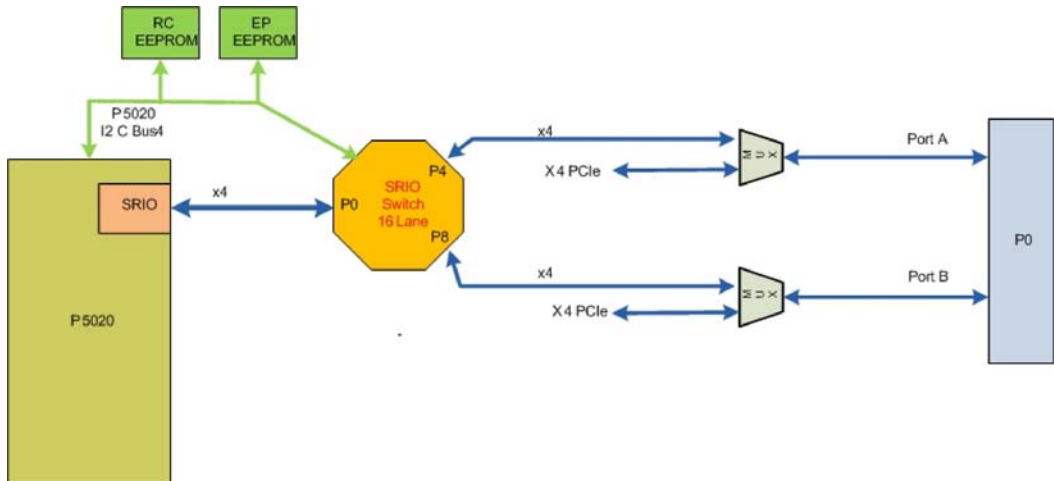
4.14 PMC/XMC Sites

The MVME8100 Series boards provide two PMC/XMC sites. Each PMC/XMC site can accept either a PMC or an XMC add-on card. For a given PMC/XMC site, only an XMC or a PMC maybe populated at any given time, as they occupy the same physical space on the PCB. The PMC/XMC1 site provides rear PMC I/O.

The PMC/XMC sites are fully compliant with the following:

- VITA 39 -PCI-X for PMC
- VITA 35-2000 for PMC P4 to VME P2 Connection (PMC/XMC1 site only)
- PCI Rev 2.2 for PCI Local Bus Specification
- PCI-X PT 2.0 for PCI-X Protocol Addendum to the PCI Local Bus Specs
- IEEE Standard P1386-2001 for Standard for Common Mezzanine Card Family
- IEEE Standard P1386.1-2001 for Standard Physical and Environmental Layer for PCI Mezzanine Card.
- VITA 42 for XMC
- VITA 42.3, PCIe for XMC

PMC/XMC sites are keyed for 3.3V PMC signaling.

MVME8100 Series boards provide a x8 PCI Express interface link for PMC/XMC1 and x4 PCI Express interface link for PMC/XMC2. It is designed such that same PCI Express interface is used for either the XMC or the PCIe to PCI-X bridge required for a PMC. This is made possible by using Pericom PI3PCIE3412 PCIe mux devices. The PCIe Mux at both sites is controlled by the CPLD. The CPLD detects the presence signal provided by the XMC or PMC board and it will be used to configure the routing of PCIe Mux accordingly.

4.14.1 PMC Add-on Card

The MVME8100 Series boards support up to two PMC cards. PCI-X operation to each site is provided using a separate IDT TSI384 PCIe to PCI-X bridge for each site. Each IDT Tsi384 can support up to 8.5 Gbps (64 bits x 133MHz). An on-board switch will configure the TSI384 to run on either 100MHz or 133MHz. The default is 133MHz.

The MVME8100 Series boards support multi-function PMCs and Processor PMCs (PrPMCs). The PCI signaling voltage (VIO) for the site is 3.3V as required by the IDT Tsi384 and is keyed as such. The power budget allocated to 3.3V is 16.5W (max) for either PMC or PrPMC. The PMC site has two IDSELs, two REQ/GNT pairs, and EREADY to support PrPMC modules as defined by VITA39.

4.14.2 XMC Add-on Card

XMC add-on cards are required to operate off of +5V or +12V (from carrier to XMC). The MVME8100 provides +5V to the XMC VPWR (Variable Power) pins. The MVME8100 Series boards do not provide +12V to the XMC VPWR pins. Voltage tolerances for VPWR and all carrier supplied voltage (+3.3V, +12V, -12V) are defined by the base XMC standard.

4.15 SATA interface

The MVME8100 Series boards are designed to support an optional 2.5 inch SATA HDD/SDD in PMC/XMC Site 2. The heat frame has mounting holes to support the 2.5" SSD/HDD on board. The connector interface to the MVME8100 Series boards are compatible with the Penguin Solutions SATA mounting kit MVME8100-HDMTKIT4, which contains a SATA adapter board, screws and mounting brackets. The SATA adapter board provides a standard SATA connector to support horizontal mounting of the HDD/SSD.

MVME8100 Series boards use Marvell's 88SE9125B1/ 88SE9125C0 SATA controller. This is a PCI Express 2.0 to dual SATA 3.0 Host Bus Adapter. It employs the latest SATA PHY technology, operating at 1.5Gbps or 3.0Gbps.

4.16 VME Support

The MVME8100 Series boards are designed to comply with VME ANSI/VITA 1.5-2003, 2eSST. The boards support most of the addressing and data transfer modes defined by the VME64, VME64x and 2eSST specifications; and can operate in System Controller (SCON) mode or in Non-SCON mode. This is determined by on board switch settings on S4.

4.16.1 Tsi148 VME Controller

The Tsi148 provides the required VME64, VME64X and 2eSST functions. TI SN74VMEH22501 transceivers buffer the VME signals between Tsi148 and the VME backplane. Refer to the *IDT Tsi148 User's Manual* for additional details and programming information.

4.16.2 Tsi384 PCIe to PCI/PCI-X Bridge

The PCIe to PCI/PCI-X Bridge function required to interface to the Tsi148 is provided by the Tsi384 device. The Tsi384 is responsible for bridging bi-directional traffic between the PCIe switch and the Tsi148. Per ANSI/VITA 1.5-2003, the theoretical maximum transfer rate for a 6U VME card in 2eSST mode is 320MBps, or 2.62Gbps.

4.17 USB

The P5020/P5010 provides two USB 2.0 controllers with integrated PHYs. The MVME8100/MVME8110 routes USB port 1 to the front panel to an upright USB Type A receptacle. The DC power for the front panel USB port is supplied through Micrel's MIC2076 power switch which provides soft, current limiting, over current detection and power enable.

The P5020/P5010 USB port 2 is routed to a USB2512 hub device which provides two additional downstream USB 2.0 ports. The two additional downstream ports are routed to the P2 connector for use on the RTM.

4.18 I^{2}C Devices

The P5020/P5010 provides four I^{2}C controllers, but only controller 1 and controller 4 are used. The I^{2}C ports are connected to multiple devices such as VPD, SPD, User EEPROMs, switch configuration EEPROMs, RTC, temperature sensors, RTM EEPROM, XMC EEPROMS, and clock devices. The RTM and XMC EEPROM addresses are configured such that they do not have an address conflict with other on board device address. The I^{2}C busses and device addresses are shown in *Figure 4-6*. For more information, refer *MVME8100 Series Programmer's Reference.*

Figure 4-6 I²C Busses
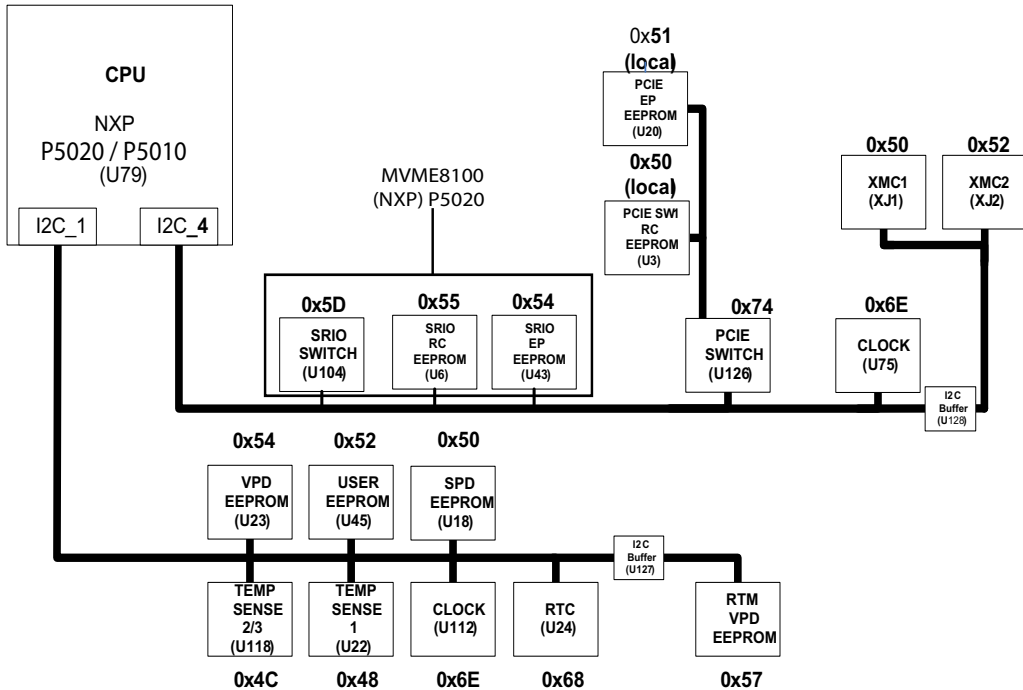
4.19 Reset/Control CPLD

The MVME8100 Series boards use a Lattice LCMXO2280C CPLD to provide reset, power up sequencing, timers, miscellaneous board logic, and status/control registers accessible through the P5020/P5010 LBC interface. The CPLD uses early 3.3V power from the +5V backplane and can be programmed through JTAG interface pins through the JTAG connector. It uses a 1.8MHz oscillator for logic control.

The CPLD provides the following functions:

- Power control and fault detection
- Reset sequence and reset management
- Status and Control registers
- Miscellaneous control logics
- Watchdog timer
- 32-bit tick timers

- Clock generator
- Switch decoder and LED controller

4.20   Power Management

The 5 volt coming from the back plane is utilized to derive all on-board voltage rails. To provide the required voltage sequencing, each voltage rail is controlled by the CPLD through enable pin of each regulator and the output is being monitored by CPLD through each regulator power good signal. If one voltage rail fails, the CPLD will disable all of the regulators and the only way to restart the board is by power cycling the chassis 5 volt power.

4.20.1 Power Distribution Structure

The following figure displays the MVME8100 Series power distribution structure.

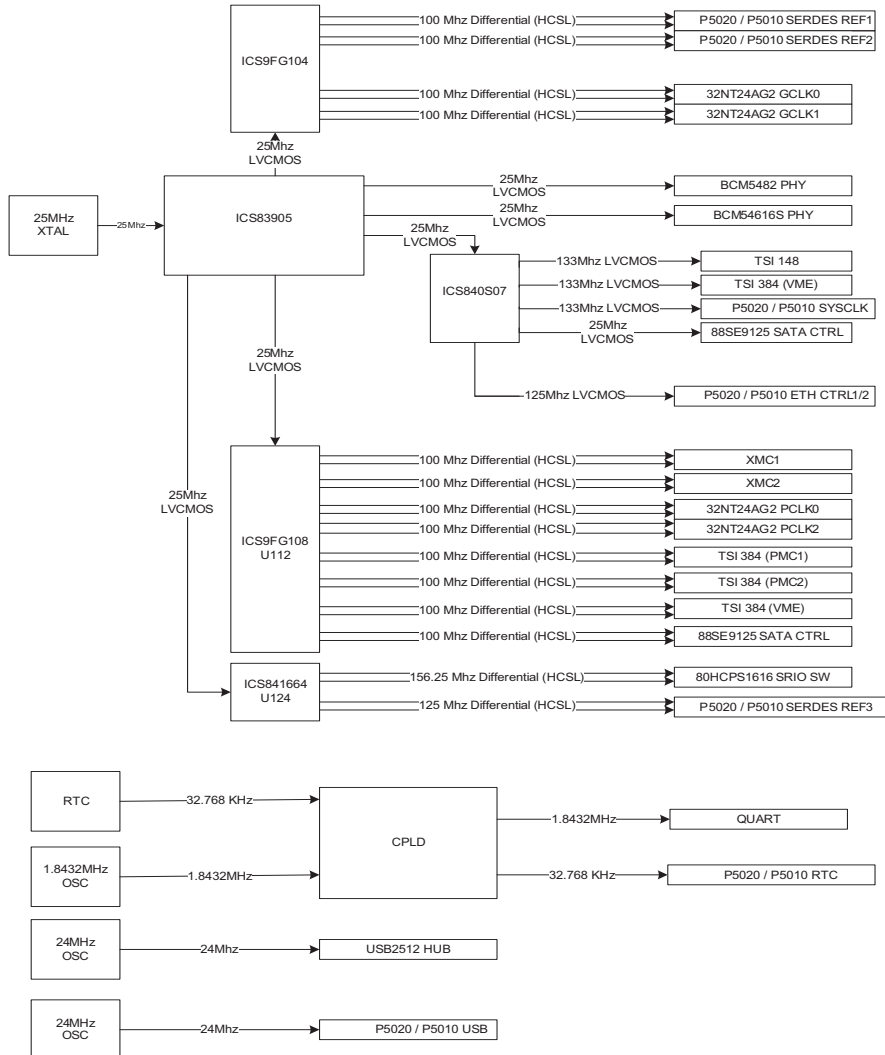*Figure 4-7 Power Distribution*
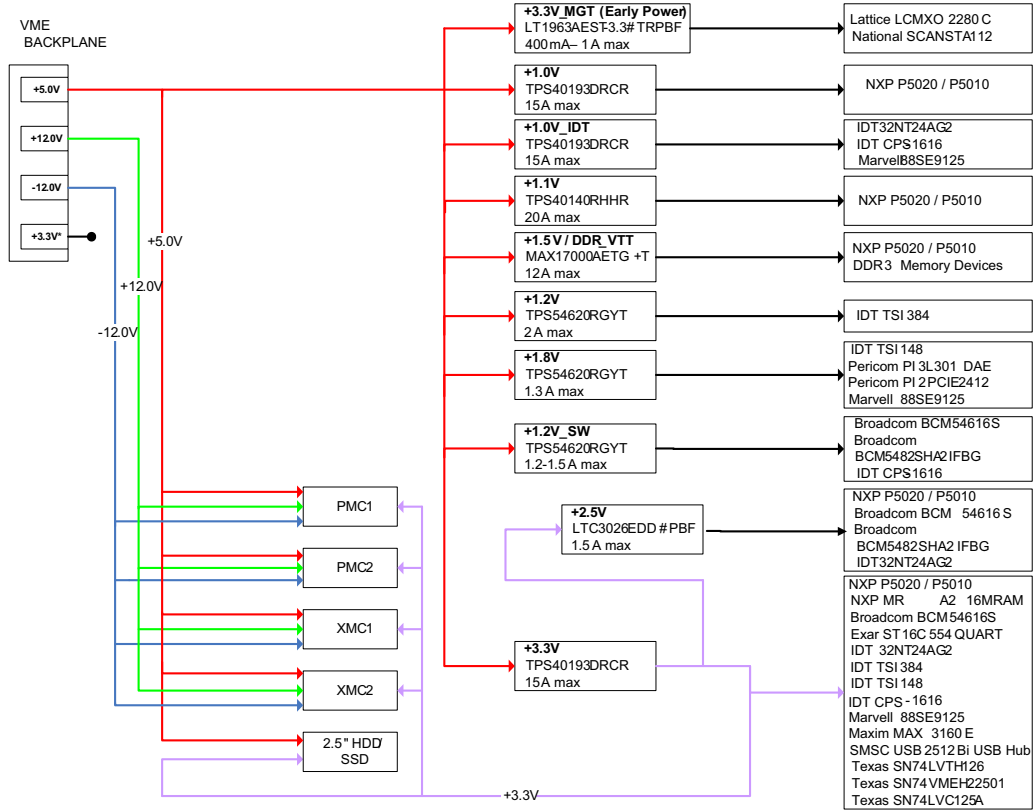
4.20.2 Power Sequence Requirements

The CPLD power sequence timing is designed to support all the MVME8100 Series devices supply voltage sequencing requirements.

4.21 Clock Structure

The figure below shows the clock tree implementation.

*Figure 4-8   Clock Structure*

4.22   Reset Structure

The MVME8100 Series reset begins after the power up sequence is completed. A board reset can also be initiated using the front panel reset switch, the RTM reset switch (through P2) or under software control through the processor Reset Request.

The following figure illustrates the reset control structure.

Figure 4-9   Reset Control Diagram
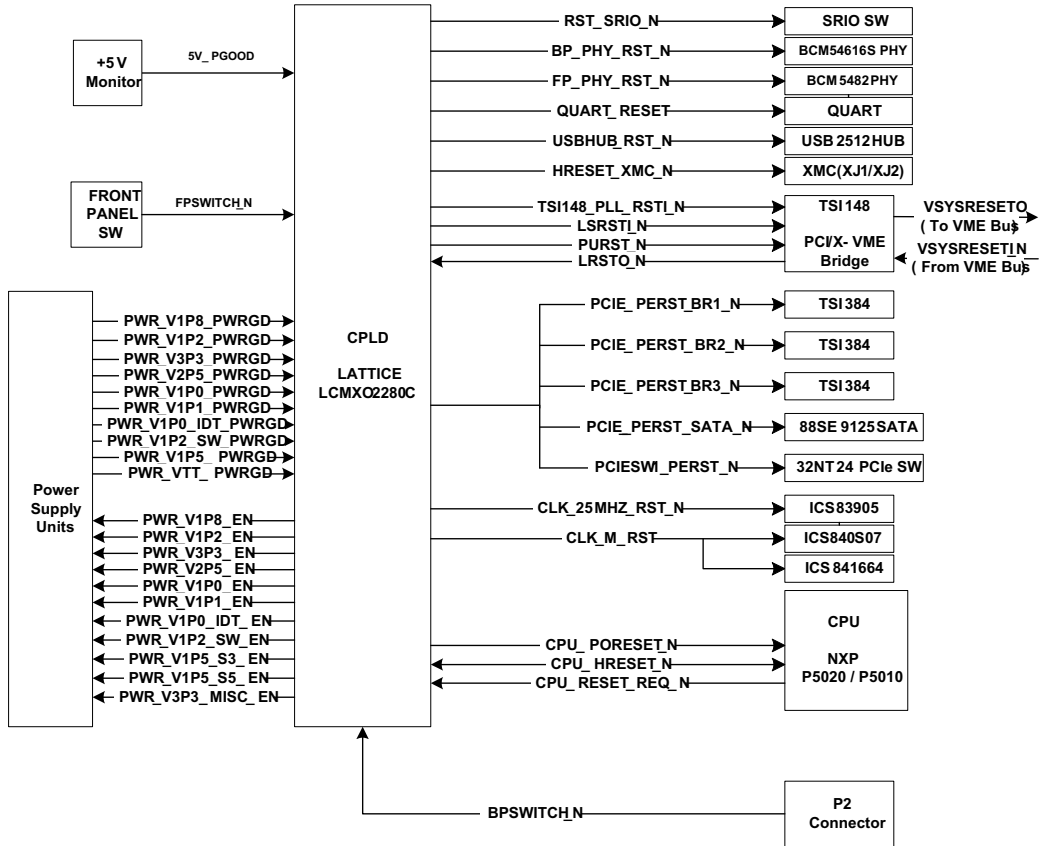
4.23   Interrupt Controller Assignments

The following table shows the external interrupts connected to the P5020 / P5010:

Table 4-1   P5020 / P5010 External Interrupt Assignments

P5020 / P5010 Interrupt	Interrupt Source	Description
IRQ0	None	Reserved
IRQ1	BCM5482 INT1	BCM5482 PHY interrupt 1 from LED_P1[2] pin
IRQ2	BCM5482 INT2	BCM5482 PHY interrupt 2 from LED_P2[2] pin
IRQ3/GPIO21	QUART_IRQ0	Quart Interrupt INTA
IRQ4/GPIO22	QUART_IRQ1	Quart Interrupt INTB
IRQ5/GPIO23	QUART_IRQ2	Quart Interrupt INTC
IRQ6/GPIO24	QUART_IRQ3	Quart Interrupt INTD
IRQ7/GPIO25	CPLD_TEMP_INT_L	Board Temperature interrupt (routed through CPLD)
IRQ8/GPIO26	CPLD_TIMER_INT_L	CPLD Internal Timers and Abort IRQ
IRQ9/GPIO27	BCM54616S INT	BCM54616S PHY interrupt from LED4 pin.
IRQ10/GPIO28	SRIO_IRQ_INT_L	80HCPS1616 SRIO IRQ_N pin (applicable to MVME8100 only)
IRQ11/GPIO29	RTC_INT_L	RTC interrupt (routed through CPLD)

IRQ10/GPIO28 with interrupt source SRIO_IRQ_INT_L is applicable to MVME8100 only.

4.24   GPIO Electrical Characteristics

The four GPIO signals routed to the P0 of MVME8100 and P2 connectors have the following electrical characteristics:

Table 4-2   GPIO DC Electrical Characteristics

V_{IL}		V_{IH}		V_{OL} Max.(V)	V_{OH} Min.(V)	I_{OL} (mA)	I_{OH} (mA)
Min.(V)	Max.(V)	Min.(V)	Max.(V)				
				0.4	2.9	4	4
-0.3	0.8	2.0	3.6	0.2	3.1	0.1	0.1

Table 4-3   GPIO Pull-Down Characteristics

Parameter	Condition	Min.	Max	Units
I/O Active Pull-down Current	V_{IL} (Max) $\leq V_{IN} \leq V_{IH}$ (Max)	30	150	uA

4.25   Thermal Management

The MVME8100 Series boards provide three on-board temperature sensors using an ADT7461 dual temperature sensor and a TMP112A temperature sensor. The ADT7461 internal temperature sensor provides the temperature at the board edge on the CPU side of the board. The ADT7461 remote temperature sensor measures the CPU temperature. The ADT7461 can measure negative temperatures down to -64°C with ±1°C accuracy on the remote sensor and ±3°C accuracy on the internal sensor. The ADT7461 registers can be used to configure the low temperature limit and high temperature limit for the local sensor as well as for the remote sensor. An interrupt can be generated if limits are exceeded. The TMP112A temperature sensor is used to measure the temperature at the board edge opposite from the CPU. Since the airflow direction can be different in some VME chassis, either temperature sensor can be used to get a measure of the board inlet air temperature, depending on the air flow direction.

However, to maintain proper CPU temperature, the recommended air flow direction is to enter the board from the CPU side, that is, the air should flow in the direction from PMC/XMC Site 1 to PMC/XMC Site 2.

Figure 4-10 Thermal Management
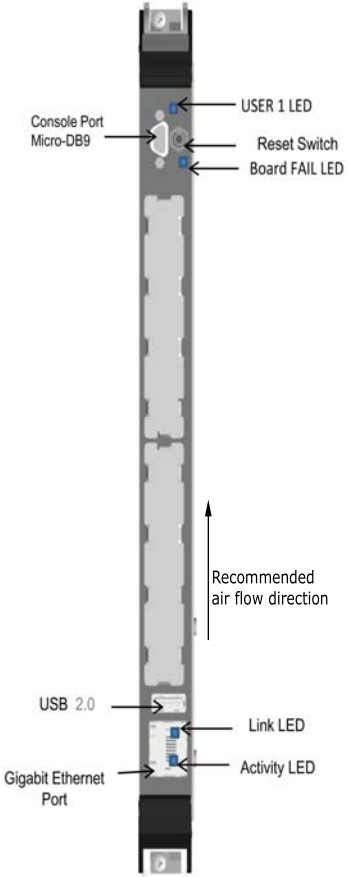
Boot System

5.1 Overview

The MVME8100 Series boards use Das U-Boot, a boot loader software based on the GNU Public License. It boots the blade and is the first software to be executed after the system is powered on.

Its main functions are:

- Initialize the hardware
- Pass boot parameters to the Linux kernel
- Start the Linux kernel
- Update Linux kernel and U-Boot images

This section describes U-Boot features and procedures that are specific to the MVME8100 Series boards. For general information on U-Boot, see *http://www.denx.de/wiki/U-Boot/WebHome*.

5.2 Accessing U-Boot

1. Connect the board to a computer with a serial interface connector and a terminal emulation software running on it. The serial connector of the board is found on the face plate.

2. Configure the terminal software to use the access parameters that are specified in U-Boot. By default, the access parameters are as follows:

   - Baud rate: 9600
   - PC ANSI
   - Eight data bits
   - No parity
   - One stop bit

> **Important Information**
>
> **These serial access parameters are the default values. These can be changed from within the U-Boot. For details, refer to the U-Boot documentation.**

3. Boot the board.

4. When prompted, press the **<Ctrl>+<C>** keys. U-Boot aborts the boot sequence and enters into a command line interface mode.

Important Information

Enter the following command to disable the U-Boot auto-boot feature and let the U-Boot directly enter the command line interface after the next reboot/power up:

```
setenv bootdelay -1; saveenv
```

5.3   Boot Options

5.3.1   Booting from a Network

In this mode, U-Boot downloads and boots the Linux kernel from an external TFTP server and mounts a root file system located on a network server.

1. Make sure that the following are accessible to the board from the TFTP server:
   ```
   kernel
   dtb
   ramdisk
   ```

2. Configure U-Boot environment variables:
   ```
   setenv ipaddr <IP address of MVME8100/MVME8110>
   setenv serverip <IP address of TFTP server>
   setenv gatewayip <gateway IP>
   setenv netmask <netmask>
   setenv bootargs 'root=/dev/ram rw console=ttyS0,9600n8
   ramdisk_size=700000 cache-sram-size=0x10000'
   saveenv
   ```

3. Transfer the files through the TFTP from the server to the local memory.
   ```
   tftp 1000000 <kernel_image>
   tftp 2000000 <ramdisk>
   tftp f00000 <kernel dtb>
   ```

4. Boot the Linux from the memory.
   ```
   bootm 1000000 2000000 f00000
   ```

5.3.2   Booting from an Optional SATA Drive

Make sure that the following are saved in the SATA drive with ext2 partition:

```
kernel
dtb
ramdisk
```

5. Configure U-Boot environment variable:

```
setenv File_uImage <kernel_image>
setenv File_dtb <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```

6. Copy the files from the SATA drive to the memory:

```
# option: scsi - interface, 0:1 - device 0 partition 1
ext2load scsi 0:1 1000000 $File_uImage
ext2load scsi 0:1 2000000 $File_ramdisk
ext2load scsi 0:1 f00000 $File_dtb
```

7. Boot the Linux in memory.

```
bootm 1000000 2000000 f00000
```

5.3.3   Booting from a USB Drive

1. Make sure that the following are saved in the USB drive with FAT partition:

```
kernel
dtb
ramdisk
```

2. Configure the U-Boot environment variable:

```
setenv File_uImage <kernel_image>
setenv File_dtb <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```

3. Initialize USB drive:

```
usb start
```

4. Load the files from the USB drive to the memory:

```
# option: usb - interface, 0:1 - device 0 partition 1
fatload usb 0:1 1000000 $File_uImage
fatload usb 0:1 2000000 $File_ramdisk
```

```
fatload usb 0:1 f00000 $File_dtb
```

5. Boot the Linux in memory:

```
bootm 1000000 2000000 f00000
```

5.3.4   Booting from eMMC

1. Make sure that the following are saved in the onboard eMMC device with FAT partition:

```
kernel
dtb
ramdisk
```

2. Configure the U-Boot environment variable:

```
setenv File_uImage <kernel_image>
setenv File_dtb <kernel dtb>
setenv File_ramdisk <ramdisk>
saveenv
```

3. Initialize eMMC

```
mmcinfo
```

4. Load the files from the eMMC to the memory:

```
# option: mmc - interface, 0:1 - device 0 partition 1
fatload mmc 0:1 1000000 $File_uImage
fatload mmc 0:1 2000000 $File_ramdisk
fatload mmc 0:1 f00000 $File_dtb
```

5. Boot the Linux in memory:

```
bootm 1000000 2000000 f00000
```

5.3.5   Booting VxWorks through the Network

In this mode, the U-Boot downloads and boots VxWorks from an external TFTP server.

1. Make sure that the VxWorks image is accessible by the board from the TFTP server.

2. Configure U-Boot environment variables:

```
ssetenv ipaddr <IP address of MVME8100/MVME8105/MVME8110>
setenv serverip <IP address of TFTP server>
setenv gatewayip <gateway IP>
setenv netmask <netmask>
etenv vxboot 'tftpboot $vxbootfile && setenv bootargs $vxbootargs
&& bootvx'
```

```
setenv vxbootfile <VxWorks_image>
setenv vxbootargs 'dtsec(3,0)<IP address of TFTP server>:VxWorks
h=<IP address of TFTP server> e=<IP address of MVME8100/MVME8105/
MVME8110>:ffffff00 b=<unused IP> u=vxworks pw=vxworks f=0x80'
saveenv
```

3. TFTP the files from the server to local memory, then boot:

```
run vxboot
```

5.4 MVME8100 Series Specific U-Boot Commands

Table 5-1   MVME8100 SeriesSpecific U-Boot Commands

Command	Description
base	Print or set address offset
bdinfo	Print board info structure
boot	Boot default, i.e., run 'bootcmd'
bootd	Boot default, i.e., run 'bootcmd'
bootelf	Boot from an ELF image in memory
bootm	Boot application image from memory
bootp	Boot image through network using BOOTP/TFTP protocol
bootvx	Boot VxWorks from an ELF image
cmp	Memory compare
coninfo	Print console devices and information
cp	Memory copy
cpu	Multiprocessor CPU boot manipulation and release
crc32	Checksum calculation
date	Get/set/reset date & time
diags	Runs POST diags
echo	Echo args to console

Table 5-1   MVME8100 SeriesSpecific U-Boot Commands (continued)

Command	Description
exit	Exit script
ext2load	Load binary file from a Ext2 file system
ext2ls	List files in a directory (default /)
fatinfo	Print information about file system
fatload	Load binary file from a DOS file system
fatls	List files in a directory (default /)
fdt	Flattened device tree utility commands
go	Start application at address 'addr'
help	Print online help
i2c	I2C sub-system
iminfo	Print header information for application image
imxtract	Extract a part of a multi-image
interrupts	Enable or disable interrupts
itest	Return true/false on integer compare
loadb	Load binary file over serial line (kermit mode)
loads	Load S-Record file over serial line
loady	Load binary file over serial line (ymodem mode)
loop	Infinite loop on address range
md	Memory display
memmap	Displays memory map
mii	MII utility commands
mm	Memory modify (auto-incrementing address)

Table 5-1   MVME8100 SeriesSpecific U-Boot Commands (continued)

Command	Description
mmc	MMC sub system
mmcinfo	Display MMC info
moninit	Reset nvram, serial#, and write monitor to SPI flash
mtest	Simple RAM read/write test
mw	Memory write (fill)
nfs	Boot image through network using NFS protocol
nm	Memory modify (constant address)
pci	List and access PCI Configuration Space
pci_info	Show information about devices on PCI bus
ping	Send ICMP ECHO_REQUEST to network host
printenv	Print environment variables
rarpboot	Boot image through network using RARP/TFTP protocol
reset	Perform RESET of the CPU
run	Run commands in an environment variable
saveenv	Save environment variables to persistent storage
script	Run a ';' delimited, ';;' terminated list of commands
scsi	SCSI sub-system
scsiboot	Boot from SCSI device
setenv	Set environment variables
setexpr	Set environment variable as the result of eval expression
sf	SPI flash sub-system
showvar	Print local hushshell variables

Table 5-1   MVME8100 SeriesSpecific U-Boot Commands (continued)

Command	Description
`sleep`	Delay execution for some time
`soft_reset`	Soft reset the board
`source`	Run script from memory
`test`	Minimal test like /bin/sh
`tftpboot`	Boot image through network using TFTP protocol
`tsi148`	Initialize and configure Tundra Tsi148
`usb`	USB sub-system
`usbboot`	Boot from USB device
`version`	Print monitor version

5.5   Updating U-Boot

To update the U-Boot, place the image in the RAM (address 0x1000000 in this example) before copying it to the SPI flash.

The following procedure will replace the image in SPI bank 0:

1. Check that the FLASH_WP_N in Surface Mount Technology (SMT) Configuration Switch (S3-1) is in the OFF position.

2. Select SPI flash # 0:
    ```
    sf probe 0
    ```

3. Erase 0x90000 bytes starting at SPI address 0:
    ```
    sf erase 0 0x90000
    ```

4. Write 0x90000 bytes from RAM address 0x1000000 starting at SPI address 0:
    ```
    sf write 0x1000000 0 0x90000
    ```

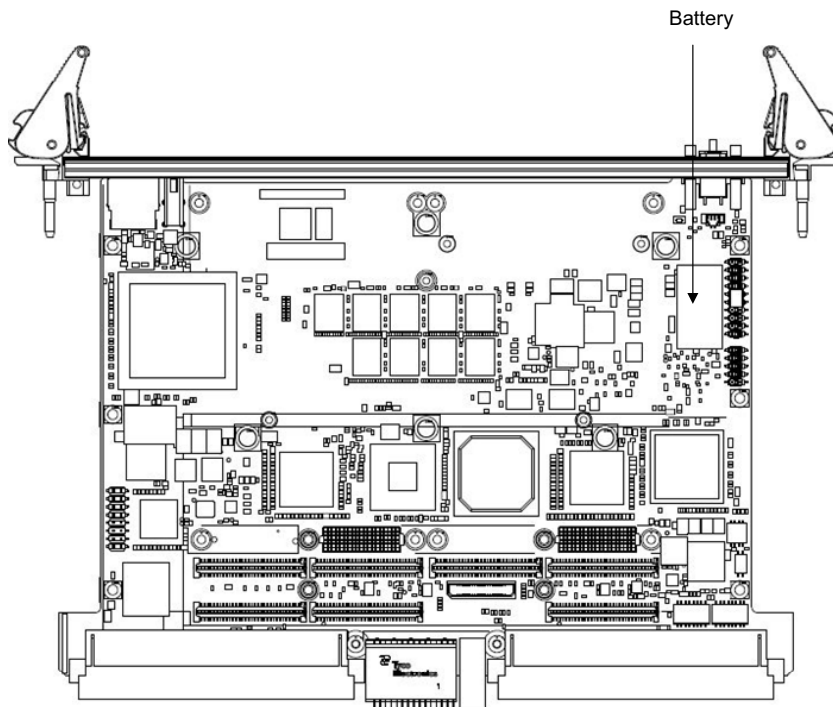To replace the image in SPI bank 1, replace step 2 with Select SPI flash # 1:
```
sf probe 1
```

Battery Exchange

A.1 Battery Exchange

The ENP1 variant contains an on-board battery. The battery location is shown in the following figure.

Figure A-1   Battery Location

The battery provides data retention of seven years summing up all periods of actual data use. Penguin Solutions therefore assumes that there usually is no need to exchange the battery except, for example, in case of long-term spare part handling.

	Data Loss
⚠	**Exchanging the battery can result in loss of time settings. Backup power prevents the loss of data during exchange.**
	Quickly replacing the battery may save time settings.
	If the battery has low or insufficient power the RTC is initialized.
	Exchange the battery before seven years of actual battery use have elapsed.

Board/System Damage

Incorrect exchange of lithium batteries can result in a hazardous explosion.

When exchanging the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models.

If the respective battery model is not available, contact your local Penguin Solutions sales representative for the availability of alternative, officially approved battery models.

PCB and Battery Holder Damage

Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

Exchange Procedure

To exchange the battery, proceed as follows:

1. Remove the old battery.

2. Install the new battery with the plus sign (+) facing up.

3. Dispose of the old battery according to your country's legislation and in an environmentally safe way.

Related Documentation

B.1   Penguin Solutions Documentation

Technical documentation can be found by using the Documentation Search at *https://www.penguinsolutions.com/edge/support/* or you can obtain electronic copies of documentation by contacting your local sales representative.

Table B-1   Penguin Edge Documentation

Document Title	Document Number
MVME8100 Data Sheet	MVME8100-DS
MVME8105 Data Sheet	MVME8105-DS
MVME8110 Data Sheet	MVME8110-DS
ProductNameLong Programmer's Reference	6806800P28
MVME8100/MVME8110 Quick start Guide	6806800P26
MVME8100/MVME8110 Safety Notes Summary	6806800P27
MVME8100/MVME8110 (VXS1-RTM1) RTM Installation and Use	6806800P46

B.2   Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2   Related Specifications

Organization and Standard	Document Title
VITA Standards Organization	
VME64	ANSI/VITA 1-1994
VME64 Extensions	ANSI/VITA 1.1-1997
2eSST Source Synchronous Transfer	ANSI/VITA 1.5-2003
Processor PMC	ANSI/VITA 32-2003
PCI-X for PMC and Processor PMC	ANSI/VITA 39-2003
XMC Switched Mezzanine Card Auxiliary Standard, September 2005	VITA 42.0-2005
XMC PCI Express Protocol Layer Standard, June 2006	VITA 42.3-2006

Organization and Standard	Document Title
Conduction Cooled PMC	ANSI/VITA 20 - 2001
PMC I/O Module (PIM) Draft Standard	VITA 36 Draft Rev 0.1 July 19, 1999
Universal Serial Bus	
Universal Serial Bus Specification	Revision 2.0 April 27, 2000
PCI Special Interest Group	
PCI Local Bus Specification, Revision 2.2	PCI Rev 2.2 December 18, 1998
PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0a	PCI-X EM 2.0a August 22, 2003
PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a	PCI-X PT 2.0a July 22, 2003
Institute for Electrical and Electronics Engineers, Inc.	
IEEE Standard for a Common Mezzanine Card (CMC) Family	IEEE1386 Oct 25, 2001
IEEE Standard Physical and Environmental Layer for PCI Mezzanine Cards: PMC	IEEE1386.1 Oct 25, 2001
Conduction cooled VME mechanics	IEEE 1101.2 - 1992
Additional Mechanical Specifications	IEEE 1101.10 - 1996
IEEE Standard for Mechanical Core Specifications for Microcomputers	IEEE 1101.1 - 1998

B.3 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-3   Manufacturer's Publications

Document Title and Source	Publication Number
NXP Corporation	
P5020/ P5010 QorIQ Integrated Processor Hardware Specifications	P5020EC
P5020 QorIQ Integrated Multicore Communication Processor Reference Manual	P5020RM
Integrated Devices	
IDT 89HPES32NT24xG2 PCI Express Switch User Manual	
CPS-1616 User Manual	

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