MVME6100 Single Board Computer

Programmer's Reference

P/N: 6806800J39C

September 2019

SMART™ Embedded Computing

Trademarks

The stylized “S” and “SMART” is a registered trademark of SMART Modular Technologies, Inc. and “SMART Embedded Computing” and the SMART Embedded Computing logo are trademarks of SMART Modular Technologies, Inc. All other names and logos referred to are trade names, trademarks, or registered trademarks of their respective owners. These materials are provided by SMART Embedded Computing as a service to its customers and may be used for informational purposes only.

Disclaimer*

SMART Embedded Computing (SMART EC) assumes no responsibility for errors or omissions in these materials. **These materials are provided “AS IS” without warranty of any kind, either expressed or implied, including but not limited to, the implied warranties of merchantability, fitness for a particular purpose, or non-infringement.** SMART EC further does not warrant the accuracy or completeness of the information, text, graphics, links or other items contained within these materials. SMART EC shall not be liable for any special, indirect, incidental, or consequential damages, including without limitation, lost revenues or lost profits, which may result from the use of these materials. SMART EC may make changes to these materials, or to the products described therein, at any time without notice. SMART EC makes no commitment to update the information contained within these materials.

Electronic versions of this material may be read online, downloaded for personal use, or referenced in another document as a URL to a SMART EC website. The text itself may not be published commercially in print or electronic form, edited, translated, or otherwise altered without the permission of SMART EC.

It is possible that this publication may contain reference to or information about SMART EC products, programming, or services that are not available in your country. Such references or information must not be construed to mean that SMART EC intends to announce such SMART EC products, programming, or services in your country.

Limited and Restricted Rights Legend

If the documentation contained herein is supplied, directly or indirectly, to the U.S. Government, the following notice shall apply unless otherwise agreed to in writing by SMART Embedded Computing.

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subparagraph (b)(3) of the Rights in Technical Data clause at DFARS 252.227-7013 (Nov. 1995) and of the Rights in Noncommercial Computer Software and Documentation clause at DFARS 252.227-7014 (Jun. 1995).

SMART Embedded Computing, Inc.

2900 S. Diablo Way, Suite 190

Tempe, Arizona 85282

USA

*For full legal terms and conditions, visit *www.smartembedded.com/ec/legal*

Table of Contents

List of Figures

Table of Contents

List of Tables

Table of Contents

About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices:

Chapter 1, Introduction on page 13, provides a brief product description and a block diagram. The remainder of the chapter provides information on memory maps and system and configuration registers.

Chapter 2, Programming Details on page 29, provides additional programming information including IDSEL mapping, interrupt assignments for the MV64360 interrupt controller, flash memory, two-wire serial interface addressing, and other device and system considerations.

Appendix A, Related Documentation on page 45, provides a listing of related SMART Embedded Computing manuals, vendor documentation, and industry specifications.

The MVME6100 Single Board Computer Programmer's Reference Guide provides general programming information, including memory maps, interrupts, and register data for the MVME6100 family of boards. This document should be used by anyone who wants general, as well as technical information about the MVME6100 products.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
AMC	Alarm Management Controller
ARP	Address Resolution Protocol
BLT	Block Transfers
CPU	Central Processing Unit
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
GB	Gigabyte
GHz	Gigahertz
IEEE	Institute of Electrical and Electronics Engineers

Abbreviation	Definition
KB	Kilobyte
LED	Light Emitting Diode
MB	Megabyte
Mbps	Megabits Per Second
MHz	Megahertz
MPP	Multi-Purpose Port
NVRAM	Non-Volatile Random Access Memory
PCI	Peripheral Component Interconnect
PCI-X	PCI Extended
RTC	Real-Time Clock
SDR	Single Data Rate
SRAM	Static Random Access Memory
TBEN	Time Base Enable
UART	Universal Asynchronous Receiver/Transmitter

Conventions

The following table describes the conventions used throughout this manual..

Notation	Description
`0x00000000`	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
`0b0000`	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands. `Sample of Programming used in a table (9pt)`
`Courier + Bold`	Used to characterize user input and to separate it from system output

Notation	Description
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	Indicates a hot surface that could result in moderate or serious injury
	Indicates an electrical situation that could result in moderate injury or death

Notation	Description
Use ESD protection 	Indicates that when working in an ESD environment care should be taken to use proper ESD practices
	No danger encountered, pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800J39C	September 2019	Re-branded to SMART Embedded Computing template. Updated Conventions table. Removed ordering table; added Ordering and Support Information.
6806800J39B	May 2014	Updated table *MVME6100 Features Summary on page 13*. Re-branded to Artesyn template.
6806800J39A	July 2009	Initial Version

Introduction

1.1 Features

This chapter briefly describes the board level hardware features of the MVME6100 single board computer, including a table of features and a block diagram. The remainder of the chapter provides memory map information including a default memory map, MOTLoad's processor memory map, a default PCI memory map, MOTLoad's PCI memory map, a PCI I/O memory map, and system I/O memory maps.

Programmable registers in the MV64360 system controller are documented in a separate publication and obtainable from your local SMART EC sales office. Refer to *Appendix A, Related Documentation*, for more information on obtaining this documentation.

The MVME6100 is a single-board computer based on the PowerPC MPC7457 processor, the Marvell MV64360 system controller, up to 2 GB of ECC-protected DDR DRAM, up to 128MB of Flash memory, a dual Gigabit Ethernet interface, two asynchronous serial ports, and two IEEE1386.1 PCI, PCI-X capable mezzanine card slots (PMCs).

The following table lists the features of the MVME6100:

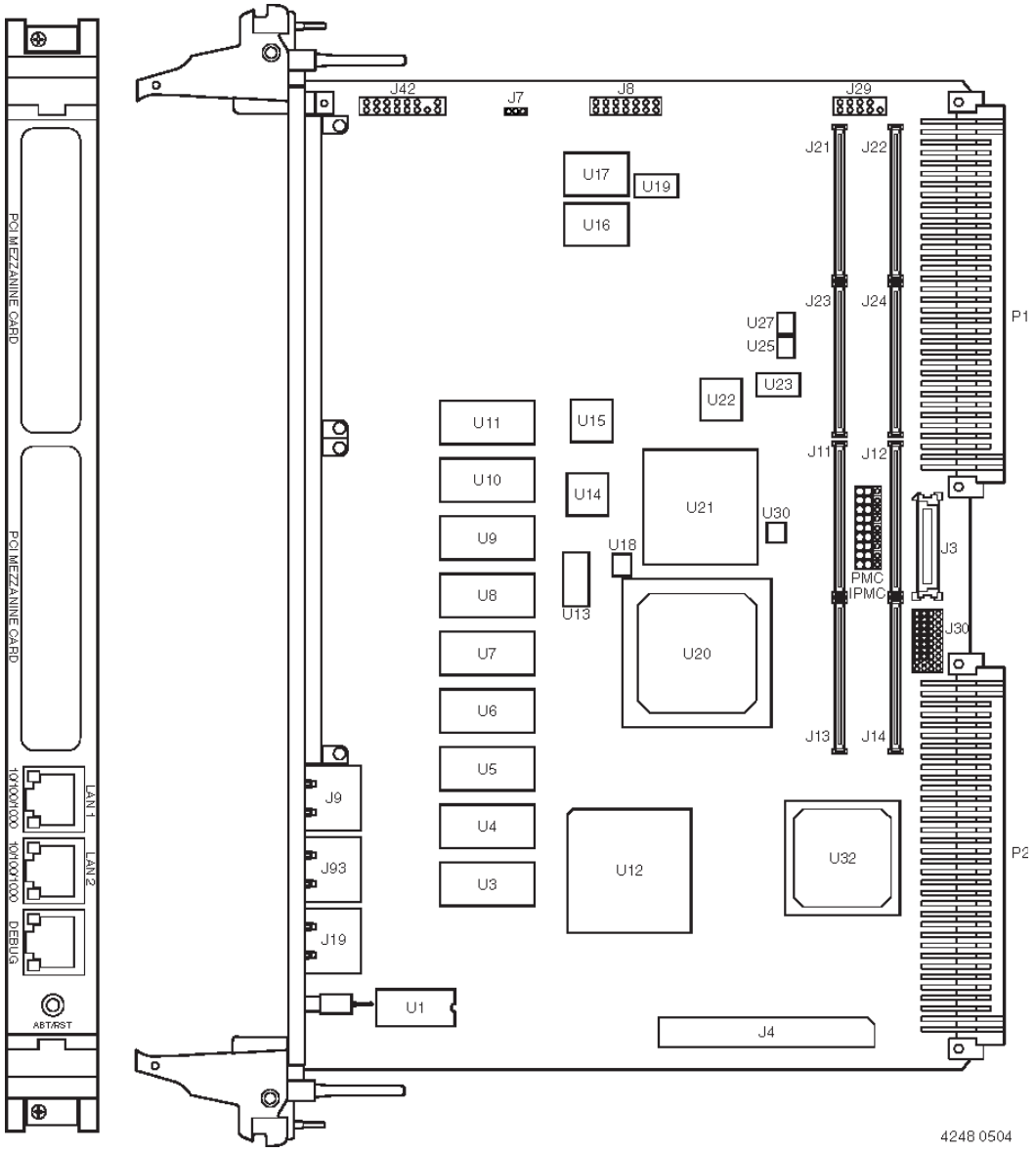
Table 1-1 MVME6100 Features Summary

Feature	Description
Processor	• Single 1.3GHz MPC7457 processor • Bus clock frequency at 133MHz • 36-bit address, 64-bit data buses • Integrated L1 and L2 cache
L3 Cache	• 2MB using SDR SRAM • Bus clock frequency at 211MHz
Flash	• Two banks (A & B) of soldered Intel StrataFlash devices • 8 to 64MB supported on each bank • Boot bank is switch selectable between banks • Bank A has combination of software and hardware write-protect scheme • Bank B top 1MB block can be write-protected through software/hardware write-protect control
System Memory	• Two banks on board for up to 2GB using 256MB or 512MB devices • Bus clock frequency at 133MHz

Table 1-1 MVME6100 Features Summary (continued)

Feature	Description
Memory Controller PCI Host Bridge Dual 10/100/1000 Ethernet Interrupt Controller PCI Interface I^2C Interface	Provided by Marvell MV64360 system controller
NVRAM Real-Time Clock Watchdog Timer	32KB provided by MK48T37
On-board Peripheral Support	• Dual 10/100/1000 Ethernet ports routed to front panel RJ-45 • connectors, one optionally routed to P2 backplane • Two asynchronous serial ports provided by an ST16C554D; one serial port is routed to a front panel RJ-45 connector and the second serial port is optionally routed to the P2 connector for rear I/O or on-board header
PCI/PMC	• Two 32/64-bit PMC slots with front-panel I/O plus P2 rear I/O as specified by IEEE P1386 • 64-bit slots; 33/66 MHz PCI or 66/100 MHz PCI-X
VME Interface	Tsi148 VME 2Esst ASIC provides: • Eight programmable VMEbus map decoders • A16, A24, A32, and A64 address • 8-bit, 16-bit, and 32-bit single cycle data transfers • 8-bit, 16-bit, 32-bit, and 64-bit block transfers • Supports SCT, BLT, MBLT, 2eVME, and 2eSST protocols • 8 entry command and 4KB data write post buffer • 4KB read ahead buffer
PMCspan Support	• One PMCspan slot • Supports 33/66 MHz, 32/64-bit PCI bus • Access through PCI6520 bridge to PMCspan
Form Factor	Standard 6U VME
Miscellaneous	• Combined reset and abort switch • Status LEDs • 8-bit software-readable switch • VME geographical address switch

Figure 1-1 MVME6100 Board Layout Diagram



1.2 Memory Maps

The section discusses the following topics:

1.2.1 Default Processor Address Map

The MV64360 presents a default CPU memory map following RESET negation. The following table shows the default memory map from the point of view of the processor. Address bits [35:32] are only relevant for the MPC7457 extended address mode and are not shown in the following tables. (Note that it is the same as the GT-64260A with the addition of integrated SRAM.)

Table 1-2 Default Processor Address Map

Processor Address				
Start	**End**	**Size**	**Definition**	**Notes**
0000 0000	007F FFFF	8M	DRAM Bank 0	
0080 0000	00FF FFFF	8M	DRAM Bank 1	
0100 0000	017F FFFF	8M	DRAM Bank 2	
0180 0000	01FF FFFF	8M	DRAM Bank 3	
0200 0000	0FFF FFFF	224M	Unassigned	
1000 0000	11FF FFFF	32M	PCI Bus 0 I/O Space	
1200 0000	13FF FFFF	32M	PCI Bus 0 Memory Space 0	
1400 0000	1BFF FFFF	128M	Unassigned	
1C00 0000	1C7F FFFF	8M	Device CS0*	
1C80 0000	1CFF FFFF	8M	Device CS1*	
1D00 0000	1DFF FFFF	16M	Device CS2*	
1E00 0000	1FFF FFFF	32M	Unassigned	

Table 1-2 Default Processor Address Map (continued)

Processor Address				
Start	**End**	**Size**	**Definition**	**Notes**
2000 0000	21FF FFFF	32M	PCI Bus 1 I/O	
2200 0000	23FF FFFF	32M	PCI Bus 1 Memory Space 0	
2400 0000	25FF FFFF	32M	PCI Bus 1 Memory Space 1	
2600 0000	27FF FFFF	32M	PCI Bus 1 Memory Space 2	
2800 0000	29FF FFFF	32M	PCI Bus 1 Memory Space 3	
2A00 0000	41FF FFFF	384M	Unassigned	
4200 0000	4303 FFFF	256K	MV64360 Integrated SRAM	
4304 0000	F0FF FFFF	2783M	Unassigned	
F100 0000	F100 FFFF	64K	Internal Registers See Note	
F101 0000	F1FF FFFF	16M-64K	Unassigned	
F200 0000	F3FF FFFF	32M	PCI Bus 0 Memory Space 1	
F400 0000	F5FF FFFF	32M	PCI Bus 0 Memory Space 2	
F600 0000	F7FF FFFF	32M	PCI Bus 0 Memory Space 3	
F800 0000	FEFF FFFF	112M	Unassigned	
FF00 0000	FF7F FFFF	8M	Device CS3*	
FC00 0000	FFFF FFFF	64M	Boot Flash (Bank A or B depending on S4:3 switch setting)	

Set by configuration resistors.

1.2.2 MOTLoad's Processor Memory Map

MOTLoad's processor memory map is given in the following table:

Table 1-3 MOTLoad's Processor Address Map

Processor Address				
Start	**End**	**Size**	**Definition**	**Notes**
0000 0000	top_dram-1	dram_size	System Memory (on-board DRAM)	
8000 0000	DFFF FFFF	536M	PCI Bus 0 and/or VME Memory Space	
E000 0000	EFFF FFFF	256M	PCI Bus 1 Memory Space	
F000 0000	F07F FFFF	8M	PCI Bus 1 I/O Space	
F080 0000	F0FF FFFF	8M	PCI Bus 0 I/O Space	
F100 0000	F10F FFFF	1M	MV64360 Internal Registers	See Note
F110 0000	F11F FFFF	1M	Device CS1* I/O System Regs/NVRAM/RTC/UARTs	
F400 0000	F7FF FFFF	64M	Device CS0* Flash Bank A	
F800 0000	FBFF FFFF	64M	Device Boot Flash Bank B	

The internal registers only occupy the first 64KB, but minimum address decoding resolution is 1MB.

1.2.3 Default PCI Memory Map

The MV64360 presents the following default PCI memory map after RESET negation. Note: it is the same as the GT-64260A with the addition of integrated SRAM.

Table 1-4 Default PCI Address Map

Processor Address				
Start	**End**	**Size**	**Definition**	**Notes**
0000 0000	007F FFFF	8M	DRAM Bank 0	
0080 0000	00FF FFFF	8M	DRAM Bank 1	
0100 0000	017F FFFF	8M	DRAM Bank 2	
0180 0000	01FF FFFF	8M	DRAM Bank 3	
0200 0000	0FFF FFFF	24M	Unassigned	
1000 0000	11FF FFFF	32M	PCI Bus 1 P2P I/O Space	
1200 0000	13FF FFFF	32M	PCI Bus 1 P2P Memory Space 0	
1400 0000	1400 FFFF	64K	Internal Registers	
1401 0000	1BFF FFFF	128M-64K	Unassigned	
1C00 0000	1C7F FFFF	8M	Device CS0*	
1C80 0000	1CFF FFFF	8M	Device CS1*	
1D00 0000	1DFF FFFF	16M	Device CS2*	
1E00 0000	1FFF FFFF	32M	Unassigned	
2000 0000	21FF FFFF	32M	PCI Bus 0 P2P I/O Space	
2200 0000	23FF FFFF	32M	PCI Bus 0 P2P Memory Space 0	
2400 0000	25FF FFFF	32M	PCI Bus 0 P2P Memory Space 1	
2600 0000	41FF FFFF	448M	Unassigned	
4200 0000	4303 FFFF	256K	MV64360 Integrated SRAM	
4304 0000	F1FF FFFF	2800M	Unassigned	
F200 0000	F3FF FFFF	32M	PCI Bus 1 P2P Memory Space 1	
F400 0000	FEFF FFFF	176M	Unassigned	
FF00 0000	FF7F FFFF	8M	Device CS3*	
FC00 0000	FFFF FFFF	64M	Boot Flash Bank B	

1.2.4 MOTLoad's PCI Memory Maps

MOTLoad's PCI memory map for each PCI domain is shown in the following table:

Table 1-5 MOTLoad's PCI Memory Maps

Processor Address				
Start	**End**	**Size**	**Definition**	**Notes**
0000 0000	top_dram	dram_size	System Memory (on-board DRAM)	

1.2.5 VME Memory Map

The MVME6100 is fully capable of supporting both the PReP and the CHRP VME Memory Map examples with RAM size limited to 2GB.

1.2.6 System I/O Memory Map

System resources including system control and status registers, NVRAM/RTC, and the 16550 UART are mapped into a 1MB address range assigned to Device Bank 1. The memory map is defined in the following table:

Table 1-6 Device Bank 1 I/O Memory Map

Address	Definition
F110 0000	System Status Register 1
F110 0001	System Status Register 2
F110 0002	System Status Register 3
F110 0003	Reserved
F110 0004	Presence Detect Register
F110 0005	Software Readable Header/Switch
F110 0006	Timebase Enable Register
F110 0008 -F110 FFFF	Reserved for on-board registers
F111 0000 -F111	7FFF M48T37V NVRAM/RTC
F112 0000 -F112 0FFF	COM 1 UART
F112 1000 -F112 0FFF	COM 2 UART
F112 2000 -F112	0FFF Reserved (undefined)
F112 3000 -F11F FFFF	Reserved (undefined)

1.2.6.1 System Status Register 1

The MVME6100 board System Status Register 1 is a read-only register used to provide board status information.

Table 1-7 System Status Register 1

REG	System Status Register 1- 0xF1100000							
BIT	7	6	5	4	3	2	1	0
FIELD	REF_CLK	BANK_SELECT	SAFE_START	ABORT_L	FLASH_BSY_L	FUSE_STAT	SROM_INIT	RSVD
OPER	R							
RESET	X	X	X	X	1	1	X	0

REF_CLK
Reference clock. This bit reflects the current state of the 28.8 KHz reference clock derived from the 1.8432 MHz UART oscillator divided by 64. This clock may be used as a fixed timing reference.

BANK_SEL
Boot Flash bank select. This bit reflects the current state of the boot Flash bank select jumper. A cleared condition indicates that Flash bank A is the boot bank. A set condition indicates that Flash B is the boot bank.

SAFE_START
ENV safe start. This bit reflects the current state of the ENV safe start select jumper. A set condition indicates that MOTLoad should provide the user the capability to select which Boot Image is used to boot the board, cleared MOTLoad should proceed with the first boot image found.

ABORT_L
Abort. This bit reflects the current state of the on-board abort signal. This is a debounced version of the abort switch and may be used to determine the state of the abort switch. A set condition indicates that the abort switch is not depressed while a cleared condition would indicate that the abort switch is asserted.

FLASH_BSY_L
FLASH Busy. This bit provides the current state of the Flash Bank A StrataFlash device Status pins. These two open drain output pins are wire ORed. Refer to the appropriate Intel StrataFlash data sheet for a description on the function of the Status pin.

FUSE_STAT
Fuse Status. This bit indicates the status of the on-board fuses. A cleared condition indicates that one of the fuses is open. A set condition indicates that all fuses are functional.

SROM_INIT
SROM Init. This bit indicates the status of the SROM Init. A cleared condition indicates that the SROM Init is disabled. A set condition indicates that the SROM Init is enabled and the MV64360 was initialized using the MV64360 User Defined Initialization SROM at $A6.

1.2.6.2 System Status Register 2

The MVME6100 board system status register 2 provides board control and status bits.

Table 1-8 System Status Register 2

REG	System Status Register 2- 0xF1100001							
BIT	7	6	5	4	3	2	1	0
FIELD	BD_FAIL	EEPROM_WP (NOT USED)	FLASHA_WP	TSTAT_MASK	FBOOTB_WP	FBA_WP_HDR	FBOOTB_WP_HDR	RSVD
OPER	R/W	R	R/W	R/W	R/W	R	R	R
RESET	1	1	1	1	1	X	X	X

BD_FAIL
Board Fail. This bit is used to control the Board Fail LED located on the front panel. A set condition illuminates the front panel LED and a cleared condition extinguishes the front panel LED.

EEPROM_WP
Not used on the MVME6100.

FLASHA_WP
Software Flash Bank A Write Protect. This bit is to provide software-controlled protection against inadvertent writes to the expansion FLASH memory devices. Clearing this bit and disabling the HW write-protect will enable writes to the Bank A Flash devices. This bit is set during reset and must be reset by the system software to enable writing of the flash devices.

TSTAT_MASK
Thermostat Mask. This bit is used to mask the DS1621 temperature sensor thermostat output. If this bit is cleared, the thermostat output will be enabled to generate an interrupt on GPP3. If the bit is set, the thermostat output is disabled from generating an interrupt.

FBOOTB_WP
Software Flash Bank B Boot Block Write Protect. This bit is to provide software-controlled protection against inadvertent writes to the Flash Bank B Top 1 MB (0xFFF00000) space. Clearing this bit and disabling HW write-protect will enable writes to the Bank B Flash Top 1MB boot block devices. This bit is set during reset and must be reset by the system software to enable writing of the Flash Bank B boot block.

FBA_WP_HDR
Hardware Flash Bank A write protect header status. Read ONLY.Hardware jumper configuration can not be overridden by the software control bit 6 in this register.

FBOOTB_WP_HDR
Hardware Flash Bank B Boot Block write protect header status. Read ONLY. Hardware jumper configuration can not be overridden by the software control bit 3 in this register.

1.2.6.3 System Status Register 3

The MVME6100 board system status register 3 provides the board software-controlled reset functions.

Table 1-9 System Status Register 3

REG	System Status Register 3- 0xF1100002							
BIT	7	6	5	4	3	2	1	0
FIELD	BOARD_RESET	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
OPER	R/W	R	R	R	R	R	R	R
RESET	0	0	0	0	0	0	0	0

BOARD_RESET
Board Reset. Setting this bit will force a hard reset of the MVME6100 board. This bit will clear automatically when the board reset is complete. This bit will always be cleared during a read.

1.2.6.4 Presence Detect Register

The MVME5500 board contains a presence detect register that may be read by the system software to determine the presence of optional devices.

Table 1-10 Presence Detect Register

REG	Presence Detect Register - 0xF1100004							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	IPMC_PRSNT	EREADY1	EREADY0	PCIE_PRSNT_L	PMC1P_L	PMC0P_L
OPER	R							
RESET	X	X	X	X	X	X	X	X

IPMC_PRSNT
IPMC Module Present. If set (HIGH true), there is PMCspan module installed. If cleared, the PMCspan module is not installed.

EREADY1
EREADY1. Indicates that the PrPMC module installed in PMC slot 2 is ready for enumeration when set. If cleared, the PrPMC module is not ready for enumeration. The PrPMC software must assert EREADY# for this bit to be set. The purpose of EREADY# is to provide a signaling method indicating that a non-monarch (vassal) PrPMC is ready to be enumerated.

EREADY0
EREADY0. Indicates that the PrPMC module installed in PMC slot 1 is ready for enumeration when set. If cleared, the PrPMC module is not ready for enumeration. The purpose of EREADY# is to provide a signaling method indicating that a non-monarch (vassal) PrPMC is ready to be enumerated.

PCIE_PRSNT_L
PMCspan Module Present. If set, there is no PMCspan module installed. If cleared, the PMCspan module is installed.

PMC0P_L
PMC Module 0 Present. If set, there is no PMC module installed in slot 0. If cleared, the PMC module is installed.

PMC1P_L
PMC Module 1 Present. If set, there is no PMC module installed in slot 1. If cleared, the PMC module is installed.

1.2.6.5 Configuration Header/Switch Register (S1)

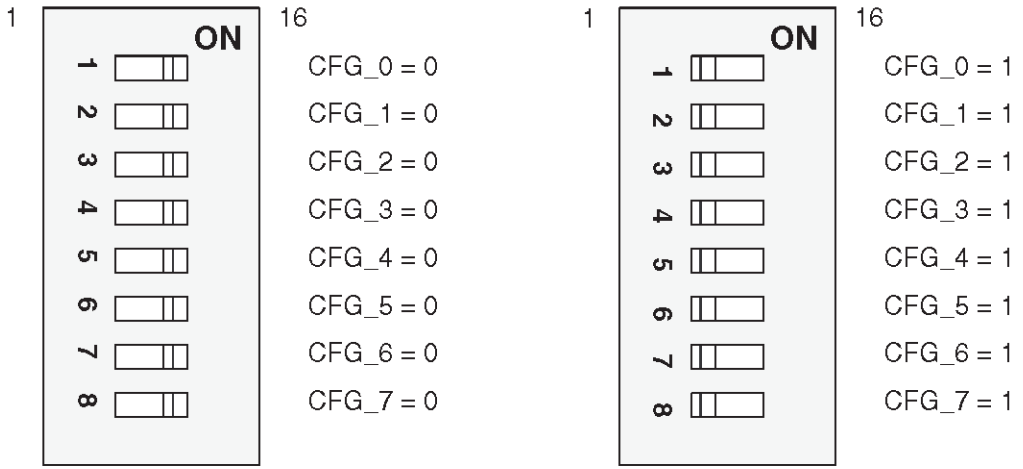
The MVME6100 board has an 8-bit header or switch that may be read by the software.

Table 1-11 Configuration Header/Switch Register

REG	Configuration Header/Switch Register - 0xF1100005							
BIT	7	6	5	4	3	2	1	0
FIELD	CFG_7	CFG_6	CFG_5	CFG_4	CFG_3	CFG_2	CFG_1	CFG_0
OPER	R							
RESET	X	X	X	X	X	X	X	X

CFG[7-0]
Configuration Bits 7-0. These bits reflect the position of the switch installed in the configuration header location. A cleared condition indicates that the switch is ON for the header position associated with that bit, and a set condition indicates that the switch is OFF.

Figure 1-2 Configuration Header/Switch Register



1.2.6.6 Time Base Enable Register

The time base enable (TBEN) register provides the means to control the processor's TBEN input.

Table 1-12 TBEN Register

REG	TBEN Register - 0xF1100006							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	TBEN1 (NOT USED)	TBEN0
OPER	R/W							
RESET	1	1	1	1	1	X	X	1

TBEN0
Processor 0 time base enable. When this bit is cleared, the TBEN pin of processor 0 is driven low. When this bit is set, the TBEN pin is driven high.

TBEN1
Not used on the MVME6100.

1.2.6.7 Quad Universal Asynchronous Receiver/Transmitter (UART)

The MVME6100 board contains one EXAR ST16C554D Quad UART device connected to the MV64360 device controller bus to provide asynchronous debug ports. The Quad UART supports up to four asynchronous serial ports of which two are used on the MVME6100. The ST16C554D is a universal asynchronous receiver and transmitter and is an enhanced UART with 16 byte FIFOs, receive trigger levels, and data rates up to 1.5 Mbps. On-board status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. The ST16C554DCQ64 provides constant active interrupt outputs but do not offer TXRDY/RXRDY outputs. Refer to the EXAR ST16C554D data sheet for additional information.

COM 1 is an RS-232 port and the TTL-level signals are routed through appropriate EIA-232 drivers and receivers to an RJ-45 connector on the front panel. COM2 is also an RS232 port which is routed to an on-board planar header for rear I/O access via option inductors/resistors. Unused control inputs on COM1 and COM2 are wired active. The reference clock frequency for the QUART is 1.8432MHz. All UART ports are capable of signaling at up to 115 Kbaud.

1.2.6.8 Real-Time Clock and NVRAM

The Real-Time Clock/NVRAM/Watchdog Timer is implemented using a SGS-Thompson M48T37V Timekeeper SRAM, and M4T28-BR12SH1 SnapHat battery. Refer to the M48T37V data sheets for additional programming information.

Table 1-13 M48T37V Access

Address Offset	Function - 0xF1110000
0x0000 - 0x5FFF	Available for users
0x0100 - 0x0200	VxWorks "bootline"
0x6000 - 0x6FFF	Reserved (MOTLoad expansion)
0x7000 - 0x7FEF	MOTLoad use (GEVs)
0x7FF0 0 0x7FFF	Real Time Block

Programming Details

2.1 Overview

This chapter includes additional programming information for the MVME6100 single board computer.

The chapter discusses the following topics:

2.1.1 MV64360 Multi-Purpose Port Configuration

The MV64360 contains a 32-bit multi-purpose port (MPP). The MPP pins can be configured as general purpose I/O pins, as external interrupt inputs, or as a specific control/status pin for one of the MV64360 internal devices. After reset, all MPP pins default to GPP pins (general purpose inputs). Software must then configure each of the pins for the desired function. The following table defines the function assigned to each MPP pin on the MVME6100 board.

Table 2-1 MV64360 MPP Pin Function Assignments

MPP Pin Number	Input/Output	Function
0	I	COM1 /COM2 interrupts (ORed)
1	I	Unused
2	I	Abort interrupt

Table 2-1 MV64360 MPP Pin Function Assignments (continued)

MPP Pin Number	Input/Output	Function
3	I	RTC and thermostat interrupts (ORed)
4	I	Unused
5	I	IPMC761 interrupt
6	I	MV64360 WDNMI# interrupt
7	I	BCM5421S PHY interrupts (ORed)
MPP[7:0] Interrupts		
8	O	PCI Bus 1 PMC slot 0 agent grant
9	I	PCI Bus 1 PMC slot 0 agent request
10	O	PCI Bus 1 PMC slot 1 agent grant
11	I	PCI Bus 1 PMC slot 1 agent request
12	O	PCI Bus 1 PMC slot 0 grant
13	I	PCI Bus 1 PMC slot 0 request
14	O	PCI Bus 1 PMC slot 1 grant
15	I	PCI Bus 1 PMC slot 1 request
MPP[15:8] PCI_1 Arbitration Request-Grant Pairs		
16	I	PCI Bus 1 Interrupts PCI-PMC0 INTA#, PMC1 INTC#
17	I	PCI Bus 1 Interrupts PCI-PMC0 INTB#, PMC1 INTD#,
18	I	PCI Bus 1 Interrupts PCI-PMC0 INTC#, PMC1 INTA#
19	I	PCI Bus 1 Interrupts PCI-PMC0 INTD#, PMC1 INTB#
20	I	PCI Bus 0 Interrupt PCI-VME INT 0 (Tempe LINT0#, PMCspan INT 2#)
21	I	PCI Bus 0 Interrupt PCI-VME INT 1 (Tempe LINT1#, PMCspan INT 3#)
22	I	PCI Bus 0 Interrupt PCI-VME INT 2 (Tempe LINT2#, PMCspan INT 0#)

Table 2-1 MV64360 MPP Pin Function Assignments (continued)

MPP Pin Number	Input/Output	Function
23	I	PCI Bus 0 Interrupt PCI-VME INT 3 (Tempe LINT3#, PMCspan INT 1#)
MPP[19:16] PCI_1 Interrupts,		
MPP[23:20] PCI_0 Interrupts		
24	O	MV64360 SROM initialization active (InitAct)
25	O	Watchdog Timer Expired output (WDE#)
26	O	Watchdog Timer NMI output (WDNMI#)
27	I	Reserved for future device interrupt
28	O	Tempe ASIC (VMEbus) grant
29	I	Tempe ASIC (VMEbus) request
30	O	PCI6520 (PMCspan bridge) grant
31	I	PCI6520 (PMCspan bridge) request
MPP[31:28] PCI_0 Arbitration Request-Grant Pairs		

2.1.2 MV64360 Reset Configuration

The MV64360 supports two methods of device initialization following reset:

- Pins sampled on the deassertion of reset
- Partial pin sample on deassertion of reset plus Serial ROM initialization via the I^2C bus for user defined initialization

The MVME6100 board supports both options. An on-board switch setting will be used to select the option. If the pin sample only method is selected, then states of the various pins on the device AD bus are sampled when reset is deasserted to determine the desired operating modes. The following table describes the configuration options. Combinations of pull ups, pull downs and switches are used to set the options. Some options are fixed and some are selectable at build time by installing the proper pull up/pull down resistor. Finally, some options may be selected using an on-board switch. Each option is described in the table.

Using the SROM initialization method, any of the MV64360 internal registers or other system components (i.e. devices on the PCI bus) can be initialized. Initialization takes place by sequentially reading 8 byte address/data pairs from the SROM and writing the 32-bit data to the decoded 32-bit address until the a data pattern matching the last serial data item register is read from the SROM (default value 0xffffffff). An 8 Kbyte EEPROM is provided on-board for this user defined initialization of the MV64360.

Table 2-2 MV64360 Power-Up Configuration Settings

Device AD Bus Signal	Select Option	Default Power-Up Setting	Description	State of Bit vs. Function	
AD[0]	Switch	X	SROM Initialization	0	No SROM initialization
				1	SROM initialization enabled
AD[1]	Resistor	1	DRAM Pads Calibration	0	Calibration Disabled
				1	Calibration Enabled
AD[3:2]	Resistors	11	SROM Device Address	00	0 1010000 ($A0)
				01	1010001 ($A2)
				10	1010010 ($A4)
				11	1010011 ($A6)
AD[4]	Fixed	1	Internal 60x Bus Arbiter	0	Internal arbiter disabled
				1	Internal arbiter enabled
AD[5]	Resistor	1	Internal Space Default Address	0	0x1400.0000
				1	0xf100.0000
AD[7:6]	Resistor	01	CPU Bus Configuration	00	60x bus mode
				01	MPX bus mode
				10	Reserved
				11	Reserved
AD[8]	Resistor	1	CPU Pads Calibration	0	Calibration Disabled
				1	Calibration Enabled
AD[9]	Fixed	0	Multiple MV64360 Support	0	Not supported
				1	Supported

Table 2-2 MV64360 Power-Up Configuration Settings (continued)

Device AD Bus Signal	Select Option	Default Power-Up Setting	Description	State of Bit vs. Function	
AD[12]	Resistor	1	PCI_0 Pads Calibration	0	Calibration Disabled
				1	Calibration Enabled
AD[13]	Resistor	1	PCI_1 Pads Calibration	0	Calibration Disabled
				1	Calibration Enabled
AD[15:14]	Resistors	10	BootCS* Device Width	00	8 bits
				01	16 bits
				10	32 bits
				11	Reserved
AD[16]	Resistor	1	PCI Retry	0	Disable
				1	Enable
AD[17	Fixed	1		1	Must pull high
AD[18]	Resistor	1	DRAM Clock Select	0	DRAM is running at a higher frequency than the core clock
				1	DRAM is running at a same frequency as the core clock
AD[19]	Resistor	1	DRAM Address/Control Delay	0	DRAM address and control signals toggle on falling edge of DRAM clock
				1	DRAM address and control signals toggle on rising edge of DRAM clock
AD[21:20]	Resistors	01	DRAM control path pipeline select	00	Reserved
				01	Two Pipe stages
				10	Reserved
				11	Three pipe stages

Table 2-2 MV64360 Power-Up Configuration Settings (continued)

Device AD Bus Signal	Select Option	Default Power-Up Setting	Description	State of Bit vs. Function	
AD[24:22]	Resistors	000	DRAM read path control	000 100	DRAM running in sync mode
				001 111	DRAM running in async mode
AD[25]	Fixed	0	Gigabit port 3 Enable	0	Disable
				1	Enable
AD[28:26]	Resistors	101	PCI_1 DLL control	000	DLL disable
				001	Conventional PCI mode at 66MHz
				101	PCI-X mode at 133 MHz
				110	PCI-X mode at 66 MHz
AD[31:29]	Resistors	101	PCI_0 DLL control	000	DLL disable
				001	Conventional PCI mode at 66MHz
				101	PCI-X mode at 133 MHz
				110	PCI-X mode at 66 MHz
TxD0[0]	Resistor	0	Gigabit port 0 GMII/PCS Select	0	MII/GMII
				1	PCS
TxD1[0]	Resistor	0	Gigabit port 1 GMII/PCS Select	0	MII/GMII
				1	PCS
WE[3:0], DP[3:0]	Resistor	X	DRAM PLL N Divider [7:4], [3:0]	TBD	Refer to MV64360 Specification MV-S100614-00 Rev. B (1/13/2003) page 144 for detail. MVME6100 is not using this mode.

Table 2-2 MV64360 Power-Up Configuration Settings (continued)

Device AD Bus Signal	Select Option	Default Power-Up Setting	Description	State of Bit vs. Function	
BADR[0]	Resistor	1	DRAM PLL NP	1	Pull up NP
BADR[1]	Resistor	1	DRAM PLL HIKVCO	1	Pull down HIKVCO
BADR[2]	Resistor	1	DRAM PLL NP	0	PLL power down (normal operation)
				1	PLL power up
TxD0[6:1]	Resistor	X	DRAM PLL M Divider	TBD	Refer to MV64360 Specification MV-S100614-00 Rev. B (1/13/2003) page 144 for detail. MVME6100 is not using this mode.
TxD0[7]	Resistor	0	JTAG Pad Calib Bypass	0	Normal Operation
				1	Bypass pad calibration
TxD1[1]	Resistor	0	Core PLL Bypass	0	Normal Operation
				1	Bypass the core's PLL
TxD1[4:2]	Resistors	000	Core PLL Control	000	Tuning of the core PLL clock tree

2.1.3 Flash Memory

The MVME6100 contains two banks of flash memory accessed via the Device Controller bus contained within MV64360. Each bank contains from 8MB to 64MB of 32-bit wide Boot Block flash memory provided by two 16-bit wide Intel StrataFlash devices.

The Boot Bank is jumper selectable to select either flash bank as the boot bank. The jumper effectively swaps the chip selects to the two flash banks so that either bank can be used as the boot bank. The state of the jumper is readable in the BANK_SELECT bit of System Status Register 1 to properly set up the MV64360 Device Controller Bus memory maps.

The boot device bank is the same as any of the other device banks except that its default address map matches the PowerPC CPU boot address (0xfff0.0100) and that its default width is sampled at reset.

2.1.4 Real-Time Clock and NVRAM

The Real-Time Clock/NVRAM/Watchdog Timer is implemented using a SGS-Thompson M48T37V Timekeeper SRAM, and M4T28-BR12SH1 SnapHat battery. Refer to the M48T37V data sheets for additional programming information. Refer to *Appendix A, Related Documentation*.

Table 2-3 M48T37V Access

Address Offset	Function - 0xF1110000
0x0000 - 0x5FFF	Available for users
0x0100 - 0x0200	VxWorks "bootline"
0x6000 - 0x6FFF	Reserved (MOTLoad expansion)
0x7000 - 0x7FEF	MOTLoad use (GEVs)
0x7FF0 0 0x7FFF	Real Time Block

2.1.5 Two-Wire Serial Interface

A two-wire serial interface for the MVME6100 is provided by an I^2C compatible serial controller integrated into the MV64360 system controller. The I^2C serial controller provides two basic functions. The first function is to provide MV64360 register initialization following a reset. The MV64360 can be configured (by switch setting) to automatically read data out of a serial EEPROM following a reset and initialize any number of internal registers. In the second function, the controller is used by the system software to read the contents of the VPD and SPD EEPROMs contained on the MVME6100 to initialize the memory controller and other interfaces. For additional details regarding the MV64360 two-wire serial controller operation, refer to the MV64360 System Controller Data Sheet. See *Appendix A, Related Documentation*.

The following table shows the I^2C devices on the MVME6100 and their assigned device IDs:

Table 2-4 I^2C Bus Device Addressing

Device Function	Size	Device Address (A2A1A0)	I^2C BUS Address	Notes
Memory SPD (Bank 0 and 1)	256 x 8	000b	$A0	1
Memory SPD (Bank 2 and 3)	256 x 8	001b	$A2	1
Reserved (PMCSpan SROM)	NA	010b	$A4	
MV64360 User Defined Initialization	8K x 8	011b	$A6	2

Table 2-4 I^2C Bus Device Addressing (continued)

Device Function	Size	Device Address (A2A1A0)	I^2C BUS Address	Notes
Configuration VPD	8K x 8	100b	$A8	2
User VPD	8K x 8	101b	$AA	2
Not Used	NA	110b	$AC	
Not Used	NA	111b	$AE	
DS1621 Temperature Sensor	NA	011b	$90	

The SPD defines the physical attributes of each bank or group of banks, i.e. if both banks of a group are populated, they will be the same speed and memory size.

This is a dual address serial EEPROM (AT24C64A or equivalent).

2.1.6 DDR DRAM Serial Presence Detect

There are two on-board SPD serial EEPROMs on the MVME6100 accessible via the I^2C serial interface. The first 128 bytes of each SPD contains module type, SDRAM organization, and timing parameters.

2.1.7 MV64360 Initialization 2

Serial EEPROM devices are provided to support optional initialization of the MV64360 (enabled by the S4:4 switch). Using the SROM initialization method, any of the MV64360 internal registers or other system components; that is, devices on the PCI bus, can be initialized. Initialization takes place by sequentially reading 8 byte address/data pairs from the SROM and writing the 32-bit data to the decoded 32-bit address until the a data pattern matching the last serial data item register is read for the SROM (default value 0xffffffff). The on-board reset logic keeps the processor reset asserted until this initialization process is completed. An SROM is provided for user MV64360 initialization.

2.1.8 VPD and User Configuration EEPROMs

The MVME6100 board contains an Atmel AT24C64 or compatible Vital Product Data (VPD) EEPROM containing configuration information specific to the board. Typical information that may be present in the VPD is: manufacturer, board revision, build version, date of assembly, memory present, options present, and L3 cache information. A second AT24C64 device is available for user data storage.

2.1.9 Temperature Sensor

The MVME6100 board provides a Maxim DS1621 digital temperature sensor with an I^2C Serial Bus interface. This device may be used to provide a measure of the ambient temperature of the board.

2.1.10 MV64360 Device Controller Bank Assignments

The MVME6100 board uses three of the MV64360 Device Controller banks for interfacing to various devices. The following tables define the device bank assignments and the programmable device bank timing parameters required for each of the banks used.

Table 2-5 Device Bank Assignments

Device Bank	Data Width	Function	Notes
0	32 bit	Bank A or Bank B Soldered FLASH	1
1	8 bit	I/O Devices	
2	NA	Not Used	
3	NA	Not Used	
Boot	32 bit	Bank A or Bank B Soldered FLASH	1

Determined by boot bank select jumper

2.1.11 MPC Bus and PCI Bus Arbitration

The MV64360 ASIC supplies these functions. Refer to the MV64360 Data Sheet, listed in *Appendix A, Related Documentation*, for details.

2.1.12 PCI Bus 0 and PCI Bus 1 Local Buses

The PCI devices on the MVME6100 are: the MV64360 ASIC, the PMCspan bridge PCI6520, the Tsi148 ASIC, PMCspan slot and the PMC Slots.

2.1.12.1 PCI Mode/Frequency Selection

The MVME6100 PCI Bus 0 bus is be set to PCI-X and 133 MHz for maximum performance. On-board logic drives the PCI-X initialization pattern, as defined by the PCI-X Addendum to the PCI Local Bus Specification Revision 1.0a at the rising edge of RST#. The MVME6100 dynamically determines the mode and frequency of the PCI Bus 1 (defined by the PCI-X Addendum to the PCI Local Bus Specification Revision 1.0b) at the rising edge of RST#. On-board logic will sense the states of PCIXCAP and M66EN for all devices on the bus and select the appropriate mode and clock frequency. Software can access the MV64360 Configuration Registers to determine the PCI mode and clock frequency of PCI Bus 1 and PCI Bus 0. Refer to the MV64360 Data Sheet, listed in *Appendix A, Related Documentation*, for details.

Voltage Input/Output (VIO) is selected on PCI Bus 1 by the position of the PMC keying pins. Both sites should be set for the same VIO; that is, keyed identically. If 5V VIO is selected, PCI Bus 1 reverts to PCI mode at 33 MHz.

2.1.12.2 PCI Configuration Space

The MV64360 controls all PCI configuration space access from either the CPU or PCI busses. The IDSEL assignments for MVME6100 are shown on the following table:

Table 2-6 IDSEL Mapping for PCI Devices

PCI Bus #	Device Number Field	PCI Address Line	IDSEL Connection
PCI Bus 0, PCI Bus 1	0b1_0000	AD16	MV64360 ASIC
PCI Bus 0,0	0b1_0100	AD22	PCI6520
PCI Bus 0	0b1_0101	AD21	Tempe VME Bridge ASIC
PCI Bus 1	0b1_0100	AD20	PMC Slot 0 (SCSI controller also uses IDSEL AD20)
PCI Bus 1	0b1_0101	AD21	PMC Slot 0, Secondary PCI Agent, IPMC slot
PCI Bus 1	0b1_0110	AD22	PMC Slot 1
PCI Bus 1	0b1_0111	AD23	PMC Slot 1, Secondary PCI Agent

2.1.12.3 PCI Arbitration Assignments for MV64360 ASIC

PCI arbitration is performed by the MV64360 ASIC. The MV64360 integrates two PCI arbiters, one for each PCI interface (PCI Bus 0/1). Each arbiter can handle up to six external agents plus one internal agent (PCI Bus 0/1 master). The internal PCI arbiter REQ#/GNT# signals are multiplexed on the MV64360 MPP pins. The internal PCI arbiter is disabled by default (the MPP pins function as general purpose inputs). Software will configure the MPP pins to function as request/grant pairs for the internal PCI arbiter.

The arbitration assignments on MVME6100 are as follows:

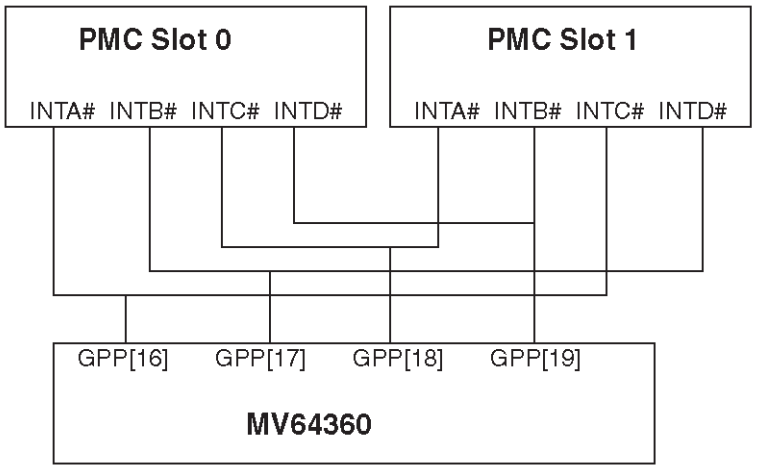
Table 2-7 PCI Arbitration Assignments for MV64360 ASIC

MPP Pin Assignment	PCI Master(s)
30, 31	PCI6520 (PMCspan bridge) GNT (MPP30), REQ (MPP 31
28, 29	Tsi148 ASIC (VMEbus) GNT (MPP 28), REQ (MPP 29)
12, 13	PMC Slot 0 GNT, REQ
14, 15	PMC Slot 1 GNT, REQ
8, 9	PMC Slot 0 Secondary PCI Agent / IPMC761 GNT, REQ
10, 11	PMC Slot 1 Secondary PCI Agent GNT, REQ

2.1.12.4 PCI Bus 1 Local Bus PMC Expansion Slots

Two PMC slots reside on the PCI Bus 1 local bus. The presence of PMCs can be positively determined by reading System Status Register 3. The INTA#, INTB#, INTC#, and INTD# from the PMC slots are routed by the MVME6100 as follows:

Figure 2-1 PCI Bus 1 Local Bus PMC Expansion Slots



2.1.12.5 PCI Bus 0 Local Bus Devices

The MV64360 PCI Bus 0 local bus contains the Tsi148 ASIC and PCI6520 PMCSpan bridge.

Tsi148 ASIC

The VMEbus interface is provided by the Tsi148 ASIC. Tempe is a PCI-X bus to VMEbus interface chip. While Tsi148 has many of the same features as the VMEchip2 and Universe, it includes new features and enhancements. Therefore, Tsi148 is not register compatible with the VMEchip2 or Universe chips. See the Tsi148 User's Manual from Tundra Semiconductor listed in *Appendix A, Related Documentation*, for further details.

PCI6520 PMCSpan Bridge

The PMCSpan interface is provided by the PCI6520. PCI6520 is a PCI-Xto- PCI-X transparent bridge to interface between PMCspan bus and the local PCI0 bus. This part operates asynchronously between primary/local PCI0 bus at 133MHz and the secondary PMCspan bus at 33 or 66MHz. See the PLX PCI6520 Specification for further programming information.

2.1.13 MV64360 Interrupt Controller

The MVME6100 uses the MV64360 interrupt controller to route internal and external interrupt requests to the CPU and the PCI bus. The MV64360 interrupt controller registers are implemented as part of the CPU interface unit in order to have minimum read latency from CPU interrupt handler. This is not backward compatible with the Discovery I implementation since the registers are placed at different offsets. The external interrupt sources will use the GPP interface to register external interrupts. The following table shows the MVME6100 interrupt assignment to MV64360 GPP pins.

Table 2-8 MV64360 Interrupt Assignments

GPP Group	MV64360	Edge/Level	Polarity	Interrupt Source	Notes
0	GPP[0]	Level	High	COM1 || COM2	3
	GPP[1]	Level	N.A.	Unused, pulled high on-board	7
	GPP[2]	Level	Low	ABORT#	
	GPP[3]	Level	Low	RTC || Thermostat output	6
	GPP[5]	Level	High	IPMC761 interrupt	2
	GPP[6]	Level	Low	MV64360 WDNMI# interrupt	
	GPP[7]	Level	Low	BCM5421S PHY 1 INTR# || BCM5421S PHY 2 INTR#	
2	GPP[16]	Level	Low	PCI-PMC 0 INTA#, PMC 1 INTC#	2
	GPP[17]	Level	Low	PCI-PMC 0 INTB#, PMC 1 INTD#,	2
	GPP[18]	Level	Low	PCI-PMC 0 INTC#, PMC 1 INTA#	2
	GPP[19]	Level	Low	PCI-PMC 0 INTD#, PMC 1 INTB#	2
	GPP[20]	Level	Low	PCI-VME INT 0 (Tsi148 LINT0#), PMCspan INT 2	1,5
	GPP[21]	Level	Low	PCI-VME INT 1 (Tsi148 LINT1#), PMCspan INT 3	1,5
	GPP[22]	Level	Low	PCI-VME INT 2 (Tsi148 LINT2#), PMCspan INT 0	1,5

Table 2-8 MV64360 Interrupt Assignments (continued)

GPP Group	MV64360	Edge/Level	Polarity	Interrupt Source	Notes
	GPP[23]	Level	Low	PCI-VME INT 3 (Tsi148 LINT3#), PMCspan INT 1	1,5
3	GPP[24]			Reserved for SROM initialization active InitAct output	
	GPP[25]			Reserved for Watchdog Timer WDE# output	
	GPP[26]			Reserved for Watchdog Timer WDNMI# output	
	GPP[27]			Reserved for future device interrupt	

The interrupting device is addressed from the MV64360 PCI Bus 0.

The interrupting device is addressed from the MV64360 PCI Bus 1.

The interrupting device is addressed from the MV64360 Device Bus.

The interrupting device is addressed from the MV64360 I^2C Bus.

The mapping of VMEbus interrupt sources and Tsi148 internal interrupt sources are programmable via the Interrupt Map Registers 1 and 2 in the Tsi148 ASIC.

The DS1621 Digital Thermometer and Thermostat provides 9-bit temperature readings which indicate the temperature of the device. The thermal alarm output, TOUT, is active when the temperature of the device exceeds a user defined temperature TH.

GPP[1,4,30,31] are unused. They are resistively pulled high on-board.

2.1.14 MV64360 Endian Issues

The MV64360 supports only a big endian CPU bus. The endianess of the local memory (DDR and SRAM) is also big endian. Data transferred to/from the local memory is never swapped. The internal registers of the MV64360 are always programed in little endian. On a CPU access to the internal registers, data is byte swapped.

Data swapping on a CPU access to the PCI is controlled via PCI Swap bits of each PCI Low Address register. This configurable setting allows a CPU access to PCI agents with a different endianess convention.

Refer to the MV64360 Data Sheet, listed in *Appendix A, Related Documentation*, for additional information and programming details.

Related Documentation

A.1 SMART Embedded Computing Documentation

The documentation listed is referenced in this manual. Technical documentation can be found by using the Documentation Search at *https://www.smartembedded.com/ec/support/* or you can obtain electronic copies of SMART EC documentation by contacting your local sales representative.

Table A-1 SMART EC Publications

Document Title	Publication Number
MVME6100 Data Sheet	MVME6100-DS
MVME6100 Single Board Computer Installation and Use	6806800D58E
MOTLoad Firmware Package User's Manual	6806800C24C
IPMC7126E/7616E I/O Module Installation and Use	6806800A45B
PMCspan PMC Adapter Carrier Board Installation and Use	

A.2 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-2 Manufacturers' Documents

Document Title and Source	Publication Number
MPC7457 RISC Microprocessor Hardware Specification *http://www.nxp.com*	MPC7457EC/D Rev. 1.3,3/2003
Tsi148 PCI/X to VME Bus Bridge User Manual *www.idt.com*	80A3020_MA001_02
PowerPC™ Apollo Microprocessor Implementation Definition Book V *http://www.nxp.com*	Addendum to SC-Vger Book IV Version - 1.0, 04/21/00
MV64360 System Controller for PowerPC Processors Data Sheet *http://www.marvell.com/*	MV-S100414-00C

Table A-2 Manufacturers' Documents (continued)

Document Title and Source	Publication Number
BCM5421S 10/100/1000BASE-T Gigabit Transceiver with SERDES Interface *http://www.broadcom.com*	5421S-DS05-D2 10/25/02
3 Volt Intel StrataFlash Memory 28F256K3 *http://www.intel.com/*	290737
PCI6520 (HB7) Transparent PCIx/PCIx Bridge Preliminary Data Book *http://www.broadcom.com*	PCI6520 Ver. 0.992
EXAR ST16C554/554D, ST68C554 Quad UART with 16-Byte FIFOs *http://www.exar.com*	ST16C554/554D Rev. 3.10
3.3V-5V 256Kbit (32Kx8) Timekeeper SRAM *http://www.st.com*	M48T37V
2-Wire Serial CMOS EEPROM *http://www.microchip.com*	AT24C02N AT24C64A
DS1621Digital Thermometer and Thermostat *http://www.maximintegrated.com/*	DS1621
TSOP Type I Shielded Metal Cover SMT *http://www.yeu.com*	

A.3 Related Specifications

For additional information, refer to the following table for related specifications. For your convenience, a source for the listed document is also provided. It is important to note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table A-3 Related Specifications

Document Title and Source	Publication Number
VITA *http://www.vita.com/*	
VME64 Specification	ANSI/VITA 1-1994
VME64 Extensions	ANSI/VITA 1.1-1997
2eSST Source Synchronous Transfer	VITA 1.5-199x

Table A-3 Related Specifications (continued)

Document Title and Source	Publication Number
PCI Special Interest Group (PCI SIG) *http://www.pcisig.com/*	
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0, 2.1, 2.2	PCI Local Bus Specification
PCI-X Addendum to the PCI Local Bus Specification	Rev 1.0b
IEEE *http://standards.ieee.org/*	
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc.	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc.	P1386.1 Draft 2.0