MVME3100 Single Board Computer

Programmer's Reference

P/N: 6806800G37C

September 2019

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About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices:

Chapter 1, Board Description and Memory Maps, provides a brief product description and a block diagram. The remainder of the chapter provides information on memory maps and system and configuration registers.

Chapter 2, Programming Details, provides additional programming information including IDSEL mapping, interrupt assignments for the MPC8540 interrupt controller, flash memory, two-wire serial interface addressing, and other device and system considerations.

Appendix A, Related Documentation, provides a listing of related SMART Embedded Computing manuals, vendor documentation, and industry specifications.

Abbreviations

Abbreviation	Description
ATA	Advanced Technology Attachment
CHRP	Common Hardware Reference Platform
CMC	Common Mezzanine Card
COM	Communication
CPU	Central Processing Unit
DDR	Double Data Rate
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
FIFO	First In First Out
GA	General Availability
GMII	Gigabit Media Independent Interface
GPCM	General Purpose Chip select Machine
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers

Abbreviation	Description
KB	Kilobytes
LBC	Local Bus Controller
LED	Light Emitting Diode
MB	Megabyte
MHz	Megahertz
MIIM	MII Management
NVRAM	Non Volatile RAM
PCI	Peripheral Connect Interface
PCI-X	Peripheral Component Interconnect -X
PHY	Physical Layer
PIC	Programmable Interrupt Controller
PIM	PCI Mezzanine Card Input/Output Module
PLD	Programmable Logic Device
PMC	PCI Mezzanine Card (IEEE P1386.1)
POR	Power-On Reset
PReP	PowerPC Reference Platform
PrPMC	Processor PMC
QUART	Quad Universal Asynchronous Receiver/Transmitter
R/W	Read/Write
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
RTM	Rear Transition Module
RTOS	Real Time Operating System
SATA	Serial AT Attachment
SBC	Single Board Computer
SDRAM	Synchronous Dynamic Random Access Memory

Abbreviation	Description
SIG	Special Interest Group
SMT	Surface Mount Technology
SPD	Serial Presence Detect
TSEC	Triple Speed Ethernet Controllers
TSOP	Thin Small Outline Package
UART	Universal Asynchronous Receiver/Transmitter
UNIX	UNIX operating system
USB	Universal Serial Bus
VIO	Input/Output Voltage
VITA	VMEbus International Trade Association
VME	VersaModule Eurocard
VMEbus	VersaModule Eurocard bus

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
`0x00000000`	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
`0b0000`	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands. `Sample of Programming used in a table (9pt)`
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury

Notation	Description
	Indicates a property damage message
	Indicates a hot surface that could result in moderate or serious injury
	Indicates an electrical situation that could result in moderate injury or death
	Indicates that when working in an ESD environment care should be taken to use proper ESD practices
	No danger encountered, pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800G37C	September 2019	Re-branded to SMART EC template
6806800G37B	May 2014	Re-branded to Artesyn template
6806800G37A	May 2008	Updated to Emerson style
V3100A/PG1		First edition

Board Description and Memory Maps

1.1 Introduction

This chapter describes the board level hardware features of the MVME3100 Single Board Computer (SBC) including a table of features and a block diagram. The remainder of the chapter provides general programming information, including memory maps, interrupts, and register data for the MVME3100 family of boards. This document should be used by anyone who wants general, as well as technical information about the MVME3100 products.

The MVME3100 is a single-slot, single-board computer based on the MPC8540 PowerQUICC III™ integrated processor. The MVME3100 provides serial ATA (SATA), USB 2.0, 2eSST VMEbus interfaces, dual 64-bit/100MHz PMC sites, up to 256MB of flash, dual 10/100/1000 Ethernet, one 10/100 Ethernet, and five serial ports. The board supports front and rear I/O and a single SODIMM module for DDR memory. Access to rear I/O is available with a rear transition module (RTM).

1.2 Ordering and Support Information

Refer to the data sheets for the MVME3100 SBC for a complete list of available variants and accessories. Refer to *Appendix A, Related Documentation on page 49* or consult your local SMART Embedded Computing sales representative for the availability of other variants.

For technical assistance, documentation, or to report product damage or shortages, contact your local SMART EC sales representative or visit *https://www.smartembedded.com/ec/support/*.

The next figure shows a block diagram of the MVME3100 and *Table 1-1* lists the features of the MVME3100.

Figure 1-1 Block Diagram

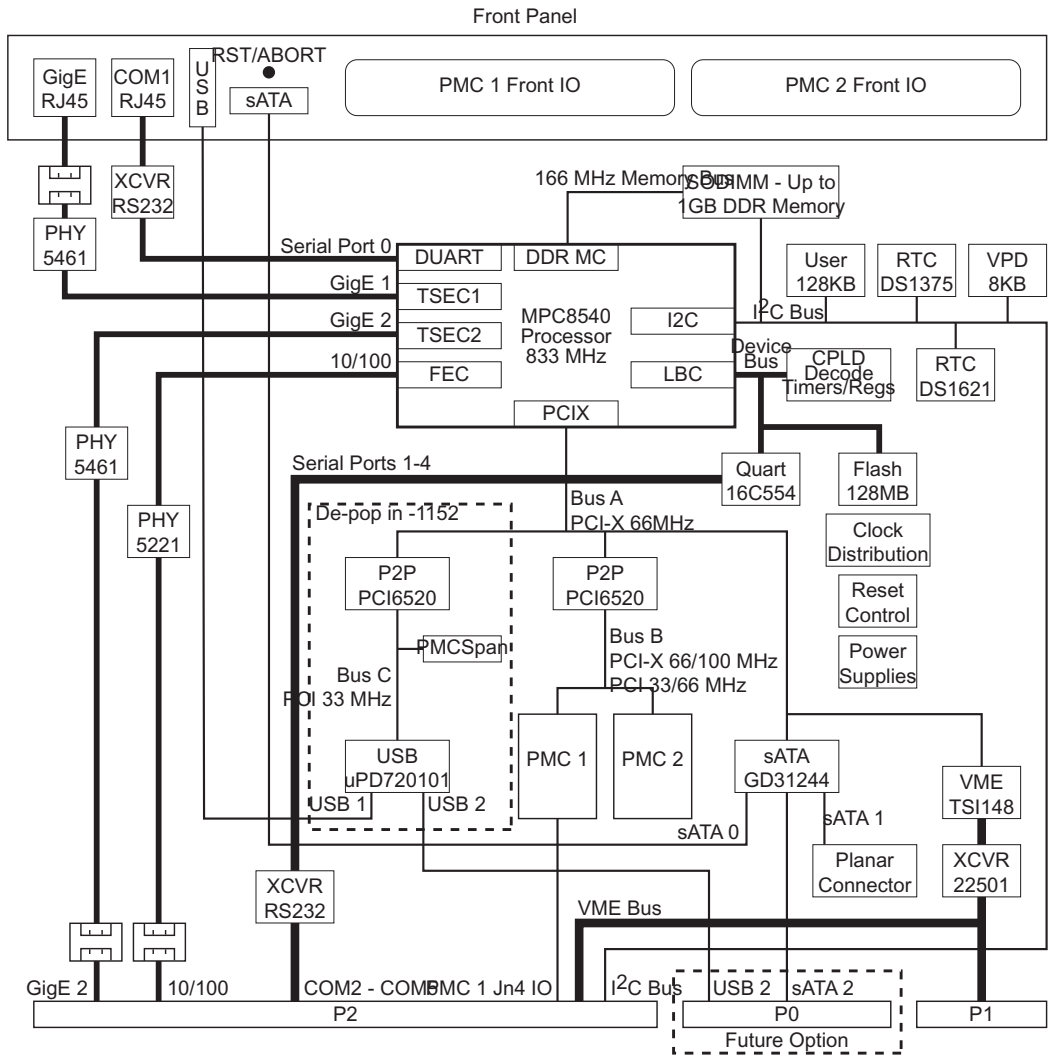

Table 1-1 MVME3100 Features Summary

Feature	Description
Processor/Host Controller/Memory Controller	– Single 667/833MHz MPC8540 PowerQUICC III™ integrated processor (e500 core) – Integrated 256KB L2 cache/SRAM – Integrated four-channel DMA controller – Integrated PCI/PCI-X controller – Two integrated 10/100/1000 Ethernet controllers – Integrated 10/100 Ethernet controller – Integrated dual UART – Integrated I2C controller – Integrated programmable interrupt controller – Integrated local bus controller – Integrated DDR SDRAM controller
System Memory	– One SODIMM socket – Up to DDR333, ECC – 256MB or 512MB SODIMM
I2C Interface	– One 8KB VPD serial EEPROM – Two 64KB user configuration serial EEPROMs – One real-time clock (RTC) with removable battery – One temperature sensor – Interface to SPD(s) on SODIMM and P2 for RTM VPD
Flash	– 32MB to 256MB soldered flash with two alternate 1MB boot sectors selectable via a hardware switch – Hardware switch or software bit write protection for entire logical bank
PCI Interface	Bus A: – 66MHz PCI-X (PCI-X 1.0b compliant) – One TSi148 VMEbus controller – One serial ATA (SATA) controller – Two PCI6520 PCI-X-to-PCI-X bridges (primary side)
	Bus B: – 33/66/100MHz PCI/PCI-X (PCI 2.2 and PCI-X 1.0b compliant) – Two +3.3V/5V selectable VIO, 64-bit, single-wide PMC sites or one double-wide PMC site (PrPMC ANSI/VITA 32-2003 and PCI-X Auxiliary ANSI/VITA 39-2003 compliant) – One PCI6520 PCI-X-to-PCI-X bridge (secondary side)
	Bus C (-1263 version): – 33MHz PCI (PCI 2.2 compliant) – One USB 2.0 controller – One PCI expansion connector for interface to PMCspan – One PCI6520 PCI-X-to-PCI-X bridge (secondary side)

Table 1-1 MVME3100 Features Summary (continued)

Feature	Description
I/O	– One front panel RJ-45 connector with integrated LEDs for front I/O: one serial channel – One front panel RJ-45 connector with integrated LEDs for front I/O: one 10/100/1000 Ethernet channel – One front panel external sATA data connector for front I/O: one sATA channel – One front panel USB Type A upright receptacle for front I/O: one USB 2.0 channel (-1263 version) – PMC site 1 front I/O and rear P2 I/O – PMC site 2 front I/O
Serial ATA	– One four-channel SATA controller: one channel for front-panel I/O, one channel for planar I/O, one channel for future rear P0 I/O, and one channel is not used – One planar data connector and one planar power connector for an interface to the sATA hard disk drive
USB (-1263 version)	– One four-channel USB 2.0 controller: one channel for front panel I/O and one channel for future rear P0 I/O. The other two channels are not used.
Ethernet	– Two 10/100/1000 MPC8540 Ethernet channels for front-panel I/O and rear P2 I/O – One 10/100 MPC8540 Ethernet channel for rear P2 I/O
Serial Interface	– One 16550-compatible, 9.6 to 115.2 KBAUD, MPC8540, asynchronous serial channel for front-panel I/O – One quad UART controller to provide four 16550-compatible, 9.6 to 115.2 KBAUD, asynchronous serial channels for rear P2 I/O
Timers	– Four 32-bit MPC8540 timers – Four 32-bit timers in a PLD
Watchdog Timer	– One MPC8540 watchdog timer
VME Interface	– VME64 (ANSI/VITA 1-1994) compliant – VME64 Extensions (ANSI/VITA 1.1-1997) compliant – 2eSST (ANSI/VITA 1.5-2003) compliant – VITA 41.0, version 0.9 compliant – Two five-row P1 and P2 backplane connectors – One TSi148 VMEbus controller
Form Factor	– Standard 6U VME

Table 1-1 MVME3100 Features Summary (continued)

Feature	Description
Miscellaneous	– One front-panel reset/abort switch – Four front-panel status indicators: 10/100/1000 Ethernet link/speed and activity, board fail, and user software controlled LED – Six planar status indicators: one power supply status LED, two user software controlled LEDs, three SATA activity LEDs (one per channel) – One standard 16-pin JTAG/COP header – Boundary scan support – Switches for VME geographical addressing in a three-row backplane
Software Support	– VxWorks operating system – Linux operating system

Table 1-2 MVME712-101 RTM Features Summary

Feature	Description
I/O	– One five-row P2 backplane connector for serial and Ethernet I/O passed from the MVME3100 – Four RJ-45 connectors for rear-panel I/O: four asynchronous serial channels – Two RJ-45 connectors with integrated LEDs for rear panel I/O: one 10/100/1000 Ethernet channel and one 10/100 Ethernet channel – One PIM site with rear-panel I/O
Miscellaneous	– Four rear-panel status indicators: 10/100/1000 and 10/100 Ethernet link/speed and activity LEDs

1.3 Memory Maps

1.3.1 Default Processor Memory Map

The MPC8540 presents a default processor memory map following RESET negation. The following table shows the default memory map from the point of view of the processor. The e500 core only provides one default TLB entry to access boot code and it allows for accesses within the highest 4KB of memory. To access the full 8MB of default boot space (and the 1MB of CCSR space), additional TLB entries must be set up within the e500 core for mapping these regions. Refer to the *MPC8540 Reference Manual* listed in *Appendix A, Related Documentation* for details.

This is the default location for the CCSRs, but it is not mapped after reset.

Table 1-3 Default Processor Address Map

Processor Address		Size	Definition	Notes
Start	End			
0000 0000	FF6F FFFF	4087M	Not mapped	
FF70 0000	FF7F FFFF	1M	MPC8540 CCS Registers	1
FF80 0000	FFFF FFFF	8M	Flash	2

Only FFFF F000 to FFFF FFFF is mapped after reset. The e500 core fetches the first instruction from FFFF FFFC following a reset.

1.3.2 MOTLoad's Processor Memory Map

MOTLoad's processor memory map is given in the following table.

Table 1-4 MOTLoad's Processor Address Map

Processor Address		Size	Definition	Notes
Start	End			
0000 0000	top_dram-1	dram_size (2GB max)	System Memory (on-board DRAM)	
8000 0000	DFFF FFFF	1.5GB	PCI Memory Space/VME	
E000 0000	E0FF FFFF	16MB	PCI I/O Space	
E100 0000	E10F FFFF	1MB	MPC8540 CCSR	
E1100 0000	E1FF FFFF	15MB	Not Used	
E200 0000	E2FF FFFF	16MB	Status/Control Registers/UARTs, External Timers	
E300 0000	EFFF FFFF	208MB	Not Used	
F000 0000	F7FF FFFF	128MB	Reserved	1, 2
bottom_flash	FFFF FFFF	flash_size (128MB max)	Flash	2

1. Reserved for future larger flash devices.

2. The flash is logically one back but may be physically implemented in two banks.

After RESET, the MPC8540 does not map any PCI memory space (inbound or outbound), and does not respond to config cycles.

1.3.3 VME Memory Map

The MVME3100 is fully capable of supporting both the PReP and the CHRP VME Memory Map examples with RAM size limited to 2GB.

1.3.4 System I/O Memory Map

System resources including System Control and Status registers, external timers, and the QUART are mapped into a 16MB address range from the MVME3100 via the MPC8540 local bus controller (LBC). The memory map is defined in the following table, including the LBC bank chip select used to decode the register:

Table 1-5 System I/O Memory Map

Address	Definition	LBC Bank / Chip Select	Notes
E200 0000	System Status Register	2	3
E200 0001	System Control Register	2	3
E200 0002	Status Indicator Register	2	3
E200 0003	Flash Control/Status Register	2	3
E200 0004	PCI Bus A Status Register	2	3
E200 0005	PCI Bus B Status Register	2	3
E200 0006	PCI Bus C Status Register	2	3
E200 0007	Interrupt Detect Register	2	3
E200 0008	Presence Detect Register	2	3
E200 0009	PLD Revision	2	3
E200 000C	PLD Date Code (32 bits)	2	3
E200 0010	Test Register 1 (32 bits)	2	3
E200 0014	Test Register 2 (32 bits)	2	3
E200 0018 - E200 0FFF	Reserved		1
E201 1000 - E201 1FFF	COM 2 (QUART channel 1)	3	
E201 2000 - E201 2FFF	COM 3 (QUART channel 2)	3	
E201 3000 - E201 3FFF	COM 4 (QUART channel 3)	3	

Table 1-5 System I/O Memory Map (continued)

Address	Definition	LBC Bank / Chip Select	Notes
E201 4000 - E201 4FFF	COM 5 (QUART channel 4)	3	
E201 5000 - E201 FFFF	Reserved		1
E202 0000	External PLD Tick Timer Prescaler Register	4	2
E202 0010	External PLD Tick Timer 1 Control Register	4	2
E202 0014	External PLD Tick Timer 1 Compare Register	4	2
E202 0018	External PLD Tick Timer 1 Counter Register	4	2
E202 001C	Reserved	4	2
E202 0020	External PLD Tick Timer 2 Control Register	4	2
E202 0024	External PLD Tick Timer 2 Compare Register	4	2
E202 0028	External PLD Tick Timer 2 Counter Register	4	2
E202 002C	Reserved	4	2
E202 0030	External PLD Tick Timer 3 Control Register	4	2
E202 0034	External PLD Tick Timer 3 Compare Register	4	2
E202 0038	External PLD Tick Timer 3 Counter Register	4	2
E202 003C	Reserved	4	2
E202 0040	External PLD Tick Timer 4 Control Register	4	2
E202 0044	External PLD Tick Timer 4 Compare Register	4	2
E202 0048	External PLD Tick Timer 4 Counter Register	4	2
E202 004C - E2FF FFFF	Reserved		1

1. Reserved for future implementation.
2. 32-bit write only.
3. Byte read/write capable.

1.3.5 System Status Register

The MVME3100 board System Status register is a read-only register used to provide board status information.

Table 1-6 System Status Register

REG	System Status Register – 0xE2000000							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	SAFE_START	ABORT	RSVD	BD_TYPE	
OPER	R							
RESET	0	0	0	X	0	0	0	0

BD_TYPE

Board type. These bits indicate the board type.

00: VME SBC
01: PrPMC
10-11: Reserved

ABORT

This bit reflects the current state of the on-board abort signal. This is a debounced version of the abort switch and may be used to determine the state of the abort switch. A cleared condition indicates the abort switch is not depressed, while a set condition indicates the abort switch is asserted.

SAFE_START

ENV safe start. This bit reflects the current state of the ENV safe start select switch. A set condition indicates that firmware should use the safe ENV settings. A cleared condition indicates that the ENV settings programmed in NVRAM should be used by the firmware.

RSVD

Reserved for future implementation.

1.3.6 System Control Register

The MVME3100 board System Control register provides board control bits.

Table 1-7 System Control Register

REG	System Control Register - 0xE2000001							
BIT	7	6	5	4	3	2	1	0
FIELD	BD_RESET			RSVD	RSVD	RSVD	EEPROM_WP	TSTAT_MASK
OPER	R/W			R	R	R	R/W	R/W
RESET	0	0	0	0	0	X	1	1

TSTAT_MASK

Thermostat mask. This bit masks the DS1621 temperature sensor thermostat output. If this bit is cleared, the thermostat output is enabled to generate an interrupt. If the bit is set, the thermostat output is disabled from generating an interrupt.

EEPROM_WPEEPROM

Write protect. This bit provides protection against inadvertent writes to the on-board EEPROM devices. Clearing this bit will enable writes to the EEPROM devices. Setting this bit write protects the devices. The devices are write protected following a reset.

BRD_RST

Board reset. These bits force a hard reset of the board. If a pattern is written in bits 5-7 where bit 7 is set, bit 6 is cleared, and bit 5 is set (101), a hard reset is generated. Any other pattern written in bits 5-7, does not generate a hard reset. These bits are cleared automatically when the board reset has been completed. These bits are always cleared during a read.

RSV

Reserved for future implementation.

1.3.7 System Indicator Register

The MVME3100 board provides a System Indicator register that may be read by the system software to determine the state of the on-board status indicator LEDs or written to by system software to illuminate the corresponding on-board LEDs.

Table 1-8 System Indicator Register

REG	System Indicator Register - 0xE2000002							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	RSVD	USR3	USR2	USR1	BRD_FAIL
OPER	R	R	R	R	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	1

BRD_FAIL

Board fail. This bit controls the board fail LED located on the front panel. A set condition illuminates the front-panel LED and a cleared condition extinguishes the front-panel LED.

USR1_LED

User LED 1. This bit controls the USR1 LED located on the front panel. A set condition illuminates the front-panel LED and a cleared condition extinguishes the front-panel LED.

USR2_LED

User LED 2. This bit controls the planar USR2 LED. A set condition illuminates the LED and a cleared condition extinguishes the LED.

USR3_LED

User LED 3. This bit controls the planar USR3 LED. A set condition illuminates the LED and a cleared condition extinguishes the LED.

RSVD

Reserved for future implementation.

1.3.8 Flash Control/Status Register

The MVME3100 provides software-controlled bank write protect and map select functions as well as boot block select, bank write protect, and activity status for the flash.

Table 1-9 Flash Control/Status Register

REG	Flash Control/Status Register - 0xE2000003							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	MAP_SEL	F_WP_SW	F_WP_HW	FBT_BLK_SEL	FLASH_RDY
OPER	R	R	R	R/W	R/W	R	R	R
RESET	0	0	0	0	1	X	X	1

FLASH_RDY

Flash ready. This bit provides the current state of the flash devices' Ready/Busy# pins. These open drain output pins from each flash device are wire OR'd to form flash ready.

FBT_BLK_SEL

Flash boot block select. This bit reflects the current state of the BOOT BLOCK B SELECT switch. A cleared condition indicates that boot block A is selected and mapped to the highest address. A set condition indicates that boot block B is selected and mapped to the highest address.

F_WP_HW

Hardware flash bank write protect switch status. This bit reflects the current state of the FLASH BANK WP switch. A set condition indicates that the entire flash bank is write protected. A cleared condition indicates that the flash bank is not write protected.

F_WP_SW

Software flash bank write protect. This bit provides software-controlled protection against inadvertent writes to the flash memory devices. A set condition indicates that the entire flash is write-protected. A cleared condition indicates that the flash bank is not write-protected, only when the hardware write-protect bit is also not set. This bit is set during reset and must be cleared by the system software to enable writing of the flash devices.

MAP_SEL

Memory map select. When this bit is cleared, the flash memory map is controlled by the Flash Boot Block Select switch. When the map select bit is set, boot block A is selected and mapped to the highest address.

RSVD

Reserved for future implementation.

1.3.9 PCI Bus Status Registers

The PCI Bus Status registers provide PCI bus configuration information for each of the PCI buses.

Table 1-10 PCI Bus A Status Register

REG	PCI Bus A Status Register - 0xE2000004							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	RSVD	PCI_A_64B	PCIX_A	PCI_A_SPD	
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	1	X	0	1

PCI_A_SPD

PCI bus A speed. Indicates the frequency of PCI bus A.
00: 33MHz
01: 66MHz
10: 100MHz
11: 133MHz

PCIX_A

PCI-X bus A. A set condition indicates that bus A is operating in PCI-X mode. A cleared condition indicates PCI mode.

PCI_A_64B

PCI bus A 64-bit. A set condition indicates that bus A is enabled to operate in 64-bit mode. A cleared condition indicates 32-bit mode.

RSVD

Reserved for future implementation.

Table 1-11 PCI Bus B Status Register

REG	PCI Bus B Status Register - 0xE2000005							
BIT	7	6	5	4	3	2	1	0
FIELD	3.3V_VIO	5.0V_VIO	ERDY2	ERDY1	PCI_B_64B	PCIX_B	PCI_B_SPD	
OPER	R	R	R	R	R	R	R	R
RESET	X	X	X	0	1	X	X	X

PCI_B_SPD:

PCI bus B speed. Indicates the frequency of PCI bus B.

00: 33MHz
01: 66MHz
10: 100MHz
11: 133MHz

PCIX_B

PCI-X bus B. A set condition indicates that bus B is operating in PCI-X mode. A cleared condition indicates PCI mode.

PCI_B_64B

PCI bus B 64-bit. A set condition indicates that bus B is enabled to operate in 64-bit mode. A cleared condition indicates 32-bit mode.

ERDY1

EREADY1. Indicates that the PrPMC module installed in PMC site 1 is ready for enumeration when set. If cleared, the PrPMC module is not ready for enumeration. If no PrPMC is installed, this bit is always set.

ERDY2

EREADY2. Indicates that the PrPMC module installed in PMC site 2 is ready for enumeration when set. If cleared, the PrPMC module is not ready for enumeration. If no PrPMC is installed, the bit is always set.

5.0V_VIO

5.0V VIO Enabled. This bit set indicates that the PMC bus (PCI bus B) is configured for 5.0V VIO.

3.3V_VIO

3.3V VIO enabled. This bit set indicates that the PMC bus (PCI bus B) is configured to 3.3V VIO.

Table 1-12 PCI Bus C Status Register

REG	PCI Bus C Status Register - 0xE2000006							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	RSVD	PCI_C_64B	PCIX_C	PCI_C_SPD	
OPER	R	R	R	R	R	R	R	R
RESET	X	X	X	0	1	X	X	X

PCI_C_SPD

PCI bus C speed. Indicates the frequency of PCI bus C.

00: 33MHz
01: 66MHz
10: 100MHz
11: 133MHz

PCIX_C

PCI-X bus C. A set condition indicates that bus C is operating in PCI-X mode. A cleared condition indicates PCI mode.

PCI_C_64B

PCI bus C 64-bit. A set condition indicates that bus C is enabled to operate in 64-bit mode. A cleared condition indicates 32-bit mode.

RSVD

Reserved for future implementation.

1.3.10 Interrupt Detect Register

The MVME3100 provides an Interrupt Detect register that may be read by the system software to determine which of the Ethernet PHYs originated their combined (OR'd) interrupt.

Table 1-13 Interrupt Detect Register

REG	Interrupt Detect Register - 0xE2000007							
BIT	7	6	5	4	3	2	1	0
FIELD	RSVD	RSVD	RSVD	RSVD	RSVD	FEC_PHY	TSEC2_PHY	TSEC1_PHY
OPER	R	R	R	R	R	R	R	R
RESET	1	1	1	0	0	0	0	0

TSEC1_PHY

TSEC1 PHY interrupt. If cleared, the TSEC1 interrupt is not asserted. If set, the TSEC1 interrupt is asserted.

TSEC2_PHY

TSEC2 PHY interrupt. If cleared, the TSEC2 interrupt is not asserted. If set, the TSEC2 interrupt is asserted.

FEC_PHY

FEC PHY interrupt. If cleared, the FEC interrupt is not asserted. If set, the FEC interrupt is asserted.

RSVD

Reserved for future implementation.

1.3.11 Presence Detect Register

The MVME3100 provides a Presence Detect register that may be read by the system software to determine the presence of optional devices.

Table 1-14 Presence Detect Register

REG	Presence Detect Register - 0xE2000008							
BIT	7	6	5	4	3	2	1	0

Table 1-14 Presence Detect Register (continued)

REG	Presence Detect Register - 0xE2000008							
FIELD	RSVD	RSVD	RSVD	RSVD	RSVD	PEP	PMC2P	PMC1P
OPER	R	R	R	R	R	R	R	R
RESET	0	0	0	0	0	X	X	X

PMC1P

PMC module 1 present. If cleared, there is no PMC module installed in site 1. If set, the PMC module is installed.

PMC2P

PMC module 2 present. If cleared, there is no PMC module installed in site 2. If set, the PMC module is installed.

PEP

PMCspan present. If cleared, there is no PMCspan module installed. If set, the PMCspan module is installed.

RSVD

Reserved for future implementation.

1.3.12 PLD Revision Register

The MVME3100 provides a PLD Revision register that may be read by the system software to determine the current revision of the timers/registers PLD.

Table 1-15 PLD Revision Register

REG	PLD Revision Register - 0xE2000009							
BIT	7	6	5	4	3	2	1	0
FIELD	PLD_REV							
OPER	R							
RESET	01							

PLD_REV

8-bit field containing the current timer/register PLD revision. The revision number starts with 01.

1.3.13 PLD Data Code Register

The MVME3100 PLD provides a 32-bit register that contains the build date code of the timers/registers PLD.

Table 1-16 PLD Data Code Register

REG	PLD Data Code Register - 0xE200000C			
BIT	31:24	23:16	15:8	7:0
FIELD	yy	mm	dd	vv
OPER	R/W			
RESET	xxxx			

yy: Last two digits of the year

mm: Month

dd: Day

vv: Version

1.3.14 Test Register 1

The MVME3100 provides a 32-bit general-purpose read/write register that can be used by software for PLD test or general status bit storage.

Table 1-17 Test Register 1

REG	Test Register 1 - 0xE2000010
BIT	31:0
FIELD	TEST1
OPER	R/W
RESET	0000

TEST1

General-purpose 32-bit read/write field.

1.3.15 Test Register 2

The MVME3100 provides a second 32-bit test register that reads back the complement of the data in test register 1.

Table 1-18 Test Register 2

REG	Test Register 2 - 0xE2000014
BIT	31:0
FIELD	TEST2
OPER	R/W
RESET	FFFF

TEST2

A read from this address returns the complement of the data pattern in test register 1. A write to this address writes the uncomplemented data to register TEST1.

1.3.16 External Timer Registers

The MVME3100 provides a set of tick timer registers for access to the four external timers implemented in the timers/registers PLD. These registers are 32-bit registers and are not byte writable. The following sections describe the external timer prescaler and control registers.

1.3.16.1 Prescalar Register

The prescaler provides the clock required by each of the four timers. The tick timers require a 1MHz clock input. The input clock to the prescaler is 25MHz. The default value is set for $E7, which gives a 1MHz reference clock for a 25MHz input clock source.

Table 1-19 Prescalar Register

REG	Prescalar Register - 0xE2020000 (8 bits of 32)							
BIT	7	6	5	4	3	2	1	0
FIELD	Prescalar Adjust							
OPER	R/W							
RESET	$E7							

Prescalar Adjust

The prescaler adjust value is determined by the following formula:
Prescaler adjust = 256 - (CLKIN/CLKOUT) where CLKIN is the input clock source in MHz and CLKOUT is the desired output clock reference in MHz.

1.3.16.2 Control Registers

The prescaler provides the clock required by each of the four timers. The tick timers require a 1MHz clock input. The input clock to the prescaler is 25MHz. The default value is set for $E7, which gives a 1MHz reference clock for a 25MHz input clock source.

Table 1-20 Tick Timer Control Registers

REG	**Tick Timer 1 Control Register - 0xE2020010 (32 bits)** **Tick Timer 2 Control Register - 0xE2020020 (32 bits)** **Tick Timer 3 Control Register - 0xE2020030 (32 bits)** **Tick Timer 4 Control Register - 0xE2020040 (32 bits)**													
BIT	31	...	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RSVD	...	RSVD	INTS	CINT	ENINT	OVF				RSVD	COVF	COC	ENC
OPER	R/W													
RESET	0	...	0	0	0	0	0	0	0	0	0	0	0	0

ENC

Enable counter. When this bit is high, the counter increments. When this bit is low, the counter does not increment.

COC

Clear counter on compare. When this bit is high, the counter is reset to 0 when it compares with the compare register. When this bit is low, the counter is not reset.

COVF

Clear overflow bits. The overflow counter is cleared when a 1 is written to this bit.

OVF

Overflow bits. These bits are the output of the overflow counter. The overflow counter is incremented each time the tick timer sends an interrupt to the local bus interrupter. The overflow counter can be cleared by writing a 1 to the COVF bit.

ENINT

Enable interrupt. When this bit is high, the interrupt is enabled. When this bit is low, the interrupt is not enabled.

CINT

Clear interrupt.

INTS

Interrupt status.

RSVD

Reserved for future implementation.

1.3.16.3 Compare Registers

The tick timer counter is compared to the Compare register. When they are equal, the tick timer interrupt is asserted and the overflow counter is incremented. If the clear-on-compare mode is enabled, the counter is also cleared. For periodic interrupts, this equation should be used to calculate the compare register value for a specific period (T):

Compare register value = T (us)

When programming the tick timer for periodic interrupts, the counter should be cleared to zero by software and then enabled. If the counter does not initially start at 0, the time to the first interrupt may be longer or shorter than expected. The rollover time for the counter is 71.6 minutes.

Table 1-21 Tick Timer Compare Registers

Tick Timer 1 Compare Register - 0xE202 0014 (32 bits) Tick Timer 2 Compare Register - 0xE202 0024 (32 bits) Tick Timer 3 Compare Register - 0xE202 0034 (32 bits) Tick Timer 4 Compare Register - 0xE202 0044 (32 bits)			
BIT	31		0
FIELD	Tick Timer Compare Value		
OPER	R/W		
RESET	0		

1.3.16.4 Counter Registers

When enabled, the tick timer Counter register increments every microsecond. Software may read or write the counter at any time.

Table 1-22 Tick Timer Counter Registers

REG	**Tick Timer 1 Counter Register - 0xE202 0018 (32 bits) Tick Timer 2 Counter Register - 0xE202 0028 (32 bits) Tick Timer 3 Counter Register - 0xE202 0038 (32 bits) Tick Timer 4 Counter Register - 0xE202 0048 (32 bits**		
BIT	31		0
FIELD	Tick Timer Counter Value		
OPER	R/W		
RESET	0		

1.3.17 Geographical Address Register

The VMEbus Status register in the TSi148 provides the VMEbus geographical address of the MVME3100. This register reflects the inverted states of the geographical address pins at the 5-row, 160-pin P1 connector.

Programming Details

2.1 Introduction

This chapter includes additional programming information for the MVME3100 single board computer. Items discussed include:

2.2 MPC8540 Reset Configuration

The MVME3100 supports the power-on reset (POR) pin sampling method for MPC8540 reset configuration. The states of the various configuration pins on the MPC8540 are sampled when reset is deasserted to determine the desired operating modes. The following table describes the configuration options and the corresponding default setting. Refer to the *MPC8540 Reference Manual* listed in *Appendix A, Related Documentation*, for additional details and/or programming information.

Table 2-1 MPC8540 Power-on Reset Configuration Settings

MPC8540 Signal	Select Option	Default Setting	Description	State of Bit vs Function [1]	
PCI_REQ64_L	PLD logic	0	PCI-32 Configuration	0	PCI/PCI-X interface is 64-bit
				1	PCI/PCI-X interface is 32-bit
PCI_GNT1_L	Resistor	0	PCI Interface I/O Impedance	0	25 ohm drivers
				1	42 ohm drivers
PCI_GNT2_L	Resistor	1	PCI Arbiter Configuration	0	Disabled on-chip PCI/PCI-X arbiter [2]
				1	Enabled on-chip PCI/PCI-X arbiter
PCI_GNT3_L	Resistor	1	PCI Debug Configuration	0	PCI debug enabled
				1	PCI operates in normal mode
PCI_GNT4_L	Switch	0	PCI/PCI-X Configuration	0	PCI-X mode
				1	PCI mode
EC_MDC	Resistor	1	TSEC Width Configuration	0	Ethernet in reduced mode (RTBI or RGMII)
				1	Ethernet in standard mode (TBI or GMII)
TSEC1_ TXD7	Resistor	0	TSEC1 Protocol Configuration	0	TSEC1 controller uses GMII protocol (RGMII if TSEC1 configured in reduced mode)
				1	TSEC1 controller uses TBI protocol (RTBI if TSEC1 configured in reduced mode)

Table 2-1 MPC8540 Power-on Reset Configuration Settings (continued)

MPC8540 Signal	Select Option	Default Setting	Description	State of Bit vs Function [1]	
TSEC1_ TXD [6:4]	Resistors	111	Boot ROM Location	000	PCI/PCI-X
				001	DDR SDRAM
				011	RapidIO
				101	Local Bus GPCM 8-bit ROM
				110	Local Bus GPCM 16-bit ROM
				111	Local Bus GPCM 32-bit ROM
TSEC2_ TXD7	Resistor	0	TSEC2 Protocol Configuration	0	TSEC2 controller uses GMII protocol (or RGMII if TSEC2 configured in reduced mode)
				1	TSEC2 controller uses TBI protocol (or RTBI if TSEC2 configured in reduced mode)
TSEC2_ TXD [6:5]	Resistors	11	Local Bus Output Hold Configuration	00	0 added buffer delays (0 added buffer delays for LALE)
				01	3 added buffer delays (1 added buffer delay for LALE)
				10	2 added buffer delays (1 added buffer delay for LALE)
				11	1 added buffer delay (0 added buffer delays for LALE)
TSEC2_ TXD [2:4]	Fixed	000	RapidIO Device ID (3 lower-order bits)	000	Unconnected Inputs
LA27	Resistor	1	CPU Boot Configuration	0	CPU boot hold off mode[3]
				1	e500 core boots without waiting for configuration by an external master

Table 2-1 MPC8540 Power-on Reset Configuration Settings (continued)

MPC8540 Signal	Select Option	Default Setting	Description	State of Bit vs Function [1]	
LA [28:31]	PLD logic	0011 for 100MHz PCI bus 0101 for 66MHz PCI bus	CCB Clock PLL Ratio (CCB Clock: SYSCLK)	0000	16:1
				0010	2:1
				0011	3:1
				0100	4:1
				0101	5:1
				0110	6:1
				1000	8:1
				1001	9:1
				1010	10:1
				1100	12:1
LWE [0:1] _L 4	Resistors	11	PCI Output Hold Configuration	00	1 added buffer delay
				01	0 added buffer delays
				10	3 added buffer delays
				11	2 added buffer delays[5]
		11	PCI-X Output Hold Configuration	00	3 added buffer delays
				01	2 added buffer delays
				10	1 added buffer delay
				11	0 added buffer delays[6]
LWE [2:3] _L	Resistors	11	MPC8540 Host/Agent Configuration	00	Agent of RapidIO and PCI/PCI-X
				01	Agent of a RapidIO
				10	Agent of a PCI/PCI-X
				11	Host of both RapidIO and PCI/PCI-X
LALE, LGPL2	Resistor	01	e500 Core Clock PLL Ratio (e500 Core: CCB Clock)	00	2:1
				01	5:2
				10	3:1
				11	7:2

Table 2-1 MPC8540 Power-on Reset Configuration Settings (continued)

MPC8540 Signal	Select Option	Default Setting	Description	State of Bit vs Function [1]	
LGPL0, LGPL1	Fixed	11	RapidIO Transmit Clock Source	00	Reserved
				01	RapidIO rcv clock is source of xmit clock
				10	RapidIO xmit clock inputs are source of xmit clock
				11	**CCB clock is source of xmit clock**
LGPL3, LGPL5	Fixed	11	Boot Sequencer Configuration	00	Reserved
				01	Boot sequencer enabled with normal I2C address mode
				10	Boot sequencer enabled with extended I2C address mode
				11	**Boot sequencer disabled**
LAD [28:31]	Resistor [7]	XX	General-Purpose POR Configuration	XX	General-purpose POR configuration vector to be placed in CPPORCR register bits
MSRCID0	Resistor	1	Memory Debug Configuration	0	Debug info from the LBC is driven on MSRCID & MDVAL pins
				1	**Debug info from the DDR SDRAM controller is driven on MSRCID & MDVAL pins**
MSRCID1	Resistor	1	DDR Debug Configuration	0	Debug info on ECC pins instead of normal ECC [8]
				1	**ECC pins function in normal mode**

1. The selected configuration settings are indicated by dark cell outlines.
2. External arbitration is required.
3. e500 core does not boot until configured by an external master.
4. Dependent on PCI/PCI-X mode configuration.
5. Required to meet 2 ns hold time requirement.
6. Meets 0.7 ns hold time requirement.

7. Local bus LAD[0:31] is sampled during POR, but only LAD[28:31] are configurable by resistor option. Software can use this value to inform the firmware or operating system about initial board configuration.
8. ECC signals from memory devices must be disconnected.

2.3 MPC8540 Interrupt Controller

The MVME3100 uses the MPC8540 integrated programmable interrupt controller (PIC) to manage locally generated interrupts. Currently defined external interrupting devices and interrupt assignments, along with corresponding edge/levels and polarities, are shown in the following table.

Table 2-2 MPC8540 Interrupt Controller

Interrupt #	Edge/Level	Polarity	Interrupt Source	Notes
0	Level	Low	VME0	
1	Level	Low	VME1/External Timers	1
2	Level	Low	VME2/sATA	
3	Level	Low	VME3/UARTs (OR'd)	2
4	Level	Low	PMCSpan/PMCs/USB	
5	Level	Low	PMCspan/PMCs	
6	Level	Low	PMCspan/PMCs	
7	Level	Low	PMCspan/PMCs	
8	Level	Low	ABORT	
9	Level	Low	Temp Sensor	
10	Level	Low	Ethernet PHYs (OR'd)	
11	Level	Low	DS1375 Alarm Interrupt	

1. External timers are implemented in a PLD.

2. External UARTs are implemented using a QUART.

Refer to the *MPC8540 Reference Manual* listed in *Appendix A, Related Documentation*, for additional details regarding the operation of the MPC8540 PIC.

2.4 Local Bus Controller Chip Select Assignments

The following table shows local bus controller (LBC) bank and chip select assignments for the MVME3100 board.

Table 2-3 LBC Chip Select Assignments

LBC Bank/ Chip Select	Local Bus Function	Size	Data Bus Width	Notes
0	Boot Flash bank	32MB - 128MB	32 bits	1
1	Optional second Flash bank	32MB - 128MB	32 bits	1
2	Control/Status registers	64KB	32 bits	2
3	Quad UART	64KB	8 bits	
4	32-bit timers	64KB	32 bits	3
5-7	Not used			

1. Flash bank size determined by VPD flash packet.

2. Control/Status registers are byte read and write capable.

3. 32-bit timer registers are byte readable, but must be written as 32 bits.

2.5 Two-Wire Serial Interface

A two-wire serial interface for the MVME3100 is provided by an I^2C compatible serial controller integrated into the MPC8540. The MPC8540 I^2C controller is used by the system software to read the contents of the various I^2C devices located on the MVME3100. The following table contains the I^2C devices used for the MVME3100 and their assigned device addresses.

Table 2-4 I2C Bus Device Addressing

I2C Bus Address	Device Address A2 A1 A0 (binary)	Size (bytes)	Device Function	Notes
$90	000	N/A	DS1621 temperature sensor	
$A0	000	256 x 8	DDR memory SPD (SODIMM module banks 1 and 2 corresponding to MPC8540 memory controller chip selects 0 and 1)	1
$A2	001		Reserved	
$A4	010	65,536 x 8	User configuration	2
$A6	011	65,536 x 8	User configuration	2

Table 2-4 I2C Bus Device Addressing (continued)

I2C Bus Address	Device Address A2 A1 A0 (binary)	Size (bytes)	Device Function	Notes
$A8	100	8192 x 8	VPD (on-board system configuration)	2
$AA	101	8192 x 8	RTM VPD (off-board configuration)	2 3
$AC	110		Reserved	
$AE	111		Reserved	
$D0	N/A	N/A	DS1375 real-time clock	

1. Each SPD defines the physical attributes of each bank or group of banks. If both banks of a SODIMM are populated they are the same speed and memory size.

2. This is a dual address serial EEPROM.

3. The device address is user selectable using switches on the RTM. The recommended address setting for the MVME3100 is $AA.

2.6 User Configuration EEPROM

The MVME3100 board provides two 64KB dual address serial EEPROMs for a total of 128KB user configuration storage. These EEPROMs are hardwired to have device IDs as shown in *Table 2-4 on page 41*, and each device ID will not be used for any other function. Refer to the *2-Wire Serial EEPROM Datasheet* listed in *Appendix A, Related Documentation*, for additional details.

2.7 VPD EEPROM

The MVME3100 board provides an 8KB dual address serial EEPROM containing vital product data (VPD) configuration information specific to the MVME3100. Typical information that may be present in the EEPROM may include: manufacturer, board revision, build version, date of assembly, memory present, options present, L2 cache information, etc. The VPD EEPROM is hardwired to have a device ID as shown in *Table 2-4 on page 41*. Refer to the *2-Wire Serial EEPROM Data Sheet* listed in *Appendix A, Related Documentation*, for additional details.

2.8 RTM VPD EEPROM

The MVME3100 board provides an 8KB dual address serial EEPROM containing VPD configuration information specific to the MVME3100 RTM. Typical information that may be present in the EEPROM may include: manufacturer, board revision, build version, date of assembly, options present, etc. The RTM VPD EEPROM device ID is user selectable with the recommended value for MVME3100 as shown in *Table 2-4 on page 41*. Refer to the*2-Wire Serial EEPROM Datasheet* listed in *Appendix A, Related Documentation*, for additional details.

2.9 Ethernet PHY Address

The assigned Ethernet PHY addresses on the MPC8540 MII management (MIIM) bus is shown in the following table.

Table 2-5 PHY Types and MII Management Bus Addresses

MPC8540 Ethernet Port	Function/Location	PHY Types	PHY MIIM Address [4:0]
TSEC1	Gigabit Ethernet port routed to front panel	BCM5461S	01
TSEC2	Gigabit Ethernet port routed to P2	BCM5461S	02
Fast Ethernet Controller	10/100 Ethernet port routed to P2	BCM5221	03

2.10 Flash Memory

The MVME3100 is designed to provide one or two physical banks of soldered-on flash memory. Each bank may be populated with two AMD Spansion MirrorBit 3.0V devices configured to operate in 16-bit mode to form a 32-bit flash bank. The flash bank connected to LBC Chip Select 0 is the boot bank and is always populated. The second flash bank connected to LBC Chip Select 1 may or may not be populated depending on flash size requirements and available flash devices. The VPD flash packet(s) will determine which banks are populated and the size of the devices. Software must program one or two LBC chip selects based on the VPD flash packet information. The following table defines the supported flash density options for each bank. The factory configuration for the MVME3100-1152 is one bank of 64MB, for the MVME3100-1263 it is one bank of 128MB.

Table 2-6 Flash Options

Flash Bank Size	Spansion Part Number	Device Size
32MB	S29GL128N	128 Mbit
64MB	S29GL256N	256 Mbit

Table 2-6 Flash Options (continued)

Flash Bank Size	Spansion Part Number	Device Size
128MB	S29GL512N	512 Mbit

A hardware flash bank write protect switch is provided on the MVME3100 to enable write protection of both physical banks. Regardless of the state of the software flash write protect bit in the Flash Control/Status register, write protection is enabled for both banks when this switch is ON. When this switch is OFF, write protection is controlled by the state of the software flash write protect bit and can only be disabled by clearing this bit in the Flash Control/Status register. Refer to *Flash Control/Status Register on page 24* for more information.

The F_WE_HW bit reflects the state of the switch and is only software readable, whereas the F_WP_SW bit supports both read and write operations.

The MVME3100 provides a dual boot option for booting from one of two separate boot images in the boot flash bank, which are referred to as boot block A and boot block B. Boot blocks A and B are each 1MB in size and are located at the top (highest address) 2 MB of the boot flash memory space. Boot block A is located at the highest 1MB block and block B is the next highest 1MB block. A flash boot block switch is used to select between boot block A and boot block B. When the switch is OFF, the flash memory map is normal and block A is selected. When the switch is ON, block B is mapped to the highest address as shown below. The MAP_SEL bit in the Flash Control/Status register can override the switch and restore the memory map to the normal configuration with block A selected. Upon RESET, this mapping reverts to the switch selection.

2.11 PCI IDSEL Definition

Each PCI device has an associated address line connected via a resistor to its IDSEL pin for configuration space accesses. The following table shows the IDSEL assignments for the PCI devices and slots on each of the PCI buses on the board, along with the corresponding interrupt assignment to the PIC external interrupt pins. Refer to the *MPC8540 Reference Manual* and *PCI6520CB Data Book* and for details on generating configuration cycles on each of the PCI busses.

Table 2-7 IDSEL and Interrupt Mapping for PCI Devices

PCI Bus	Device Number Field	AD Line for IDSEL	PCI Device or Slot	Device/Slot INT to MPC8540 Ext IRQ			
				INTA#	INTB#	INTC#	INTD#
A (8540) (See Note following table)	0b0_0000	internal	MPC8540				

Table 2-7 IDSEL and Interrupt Mapping for PCI Devices (continued)

PCI Bus	Device Number Field	AD Line for IDSEL	PCI Device or Slot	Device/Slot INT to MPC8540 Ext IRQ			
				INTA#	INTB#	INTC#	INTD#
	0b0_0001	17	TSi148 VME	IRQ0	IRQ1	IRQ2	IRQ3
	0b0_0010	18	PCI6520-1				
	0b0_0011	19	PCI6520-2				
	0b0_0100	20	GD31244 sATA	IRQ2			
B (PCI6520-1)	0b0_0000	16	PMC1 Primary	IRQ4	IRQ5	IRQ6	IRQ7
	0b0_0001	17	PMC1 Secondary	IRQ5	IRQ6	IRQ7	IRQ4
	0b0_0010	18	PMC2 Primary	IRQ6	IRQ7	IRQ4	IRQ5
	0b0_0011	19	PMC2 Secondary	IRQ7	IRQ4	IRQ5	IRQ6
C (PCI6520-2)	0b0_0000	16	uPD740101 USB	IRQ4	IRQ5	IRQ6	
	0b0_0100	20	21150 on PMCSpan				
PCI Expansion (21150)	0b0_0010	18	PMCSpan Slot 1	IRQ6	IRQ7	IRQ4	IRQ5
	0b0_0011	19	PMCSpan Slot 2	IRQ7	IRQ4	IRQ5	IRQ6
	0b0_0100	20	PMCSpan Slot 3	IRQ4	IRQ5	IRQ6	IRQ7
	0b0_0101	21	PMCSpan Slot 4	IRQ5	IRQ6	IRQ7	IRQ4

The Device Number is as listed when Bus A is in PCI-X mode. If Bus A is in PCI mode, add 0x16 (0b1_0000) to the listed Device Number.

The following table shows the Vendor ID and the Device ID for each of the planar PCI devices on the MVME3100.

Table 2-8 Planar PCI Device Identification

Function	Device	Vendor ID	Device ID
System Controller	MPC8540	0x1057	0x0008
PCI-X-to-PCI-X Bridge	PCI6520CB	0x10B5	0x6520
VME Controller	TSi148	0x10E3	0x0148
sATA Controller	GD31244	0x8086	0x3200
USB Controller	µPD720101	0x1033	0x0035

2.12 PCI Arbitration Assignments

The integrated PCI/X arbiters internal to the MPC8540 and the PCI6520 bridges provide PCI arbitration for the MVME3100. The MPC8540 provides arbitration support for itself and the four PCI-X devices on PCI bus A.

The PCI6520 secondary PCI/X interface arbiters support external bus masters in addition to the PCI6520. One secondary arbiter provides arbitration for the PMC sites on PCI bus B, and the other provides arbitration for the PMCspan and USB host controller on PCI bus C.

The arbitration assignments on the MVME3100 are shown in the follow table so that software may set arbiter priority assignments if necessary.

Table 2-9 PCI Arbitration Assignments

PCI Bus	Arbitration Assignment	PCI Master(s)
A	MPC8540 PCI_REQ/GNT[0]	sATA Controller
A	MPC8540 PCI_REQ/GNT[1]	TSI148 VME Controller
A	MPC8540 PCI_REQ/GNT[2]	PCI6520 (Bus A to Bus B bridge)
A	MPC8540 PCI_REQ/GNT[3]	PCI6520 (Bus A to Bus C bridge)
B	PCI6520-1 S_REQ/GNT[0]	PMC site 1 primary master
B	PCI6520-1 S_REQ/GNT[1]	PMC site 1 secondary master
B	PCI6520-1 S_REQ/GNT[2]	PMC site 2 primary master
B	PCI6520-1 S_REQ/GNT[3]	PMC site 2 secondary master
C	PCI6520-2 S_REQ/GNT[0]	USB Controller
C	PCI6520-2 S_REQ/GNT[1]	PMCspan

2.13 Clock Distribution

The clock function generates and distributes all of the clocks required for system operation. The clock tree is designed in such a manner as to maintain the strict edge-to-edge jitter and low clock-to-clock skew required by the devices. Additional clocks required by individual devices are generated near the devices using individual oscillators. Table 2-10 on page 54 lists the clocks required on the MVME3100 along with their frequency and source. The clock tree A frequencies on bus A have a default configuration of 66 MHz. The 33/66/100 MHz clocks are dynamically configured at reset depending on the state of the PCIXCAP and M66EN pins on bus B.

The PCI clock trees A, B, and C are not required to be synchronized with each other.

Table 2-10 Clock Assignments

Device	Clock Signal(s)	Frequency (MHz)	Clock Tree Source	Qty	VIO
MPC8540	CLK_8540	66/100	A	1	3.3V
TSi148	CLK_VME	66/100	A	1	3.3V
sATA	CLK_SATA	66/100	A	1	3.3v
PCI6520 Primary	CLK_P2P_ABP	66/100	A	2	3.3V
	CLK_P2P_ACP				
PMC1	CLK_PMC1	33/66/100	B	1	3.3V
PMC2	CLK_PMC2	33/66/100	B	1	3.3V
PCI6520 Secondary	CLK_P2P_ABS	33/66/100	B	1	3.3V
	CLK_P2P_ACS	33	C	1	3.3V
USB	CLK_USB	33	C	1	3.3V
PMCspan	CLK_SPAN	33	C	1	3.3V
MPC9855	CLK66	25	Oscillator	2	3.3V
BCM5461S	CLK25_25V_PHY	25	Oscillator/ Buffer	2	2.5V
BCM5221	CLK25_33V_PHY	25	Oscillator/ Buffer	1	3.3V
Control and Timers PLD	CLK25_33V_PLD	25	Oscillator/ Buffer	1	3.3V
	CLK_LBC	CCB_CLK/8 (333 MHz/8)	MPC8540	1	3.3V
QUART	CLK_UART	1.8432	Oscillator	1	3.3V

Table 2-10 Clock Assignments (continued)

Device	Clock Signal(s)	Frequency (MHz)	Clock Tree Source	Qty	VIO
sATA	CLK37	37.5	Oscillator	1	3.3V
USB	CLK48	48	Oscillator	1	3.3V
RTC	CLK32	32.768 kHz	Crystal	1	3.3V

2.14 MPC8540 Real-Time Clock Input

The MPC8540 real-time clock (RTC) input is driven by a 1MHz clock generated by the control and timers PLD. This provides a fixed clock reference for the RTC that software can use as a known timing reference. To select this 1MHz clock as the RTC timer reference, software must set the SEL_TBCLK bit in the MPC8540 HID0 register.

2.15 MPC8540 LBC Clock Divisor

The MPC8540 LBC clock output is used by the control and timers PLD. The LBC clock is derived from a divide by 2, 4 or 8 ratio of the internal CCB (core complex bus) clock as determined by the clock ratio register (LCRR[CLKDIV]). For proper operation of the local bus, CLKDIV must be set for divide by 8, which is the default value. The software must leave this register configured for divide by 8 during initialization.

Related Documentation

A.1 SMART Embedded Computing Documentation

The documentation listed is referenced in this manual. Technical documentation can be found by using the Documentation Search at *https://www.smartembedded.com/ec/support/* or you can obtain electronic copies of SMART EC documentation by contacting your local sales representative.

Table A-1 SMART EC Documents

Document Title	Publication Number
MVME3100 Single Board Computer Installation and Use Guide	6806800M28
MVME3100 NXP® MPC8540 VME SBC	MVME3100-DS
MOTLoad Firmware Package User's Manual	6806800C24
PMCspan PMC Adapter Carrier Board Installation and Use	PMCSPANA/IH

A.2 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-2 Manufacturers' Documents

Document Title and Source	Publication Number
MPC8540 Integrated Processor Hardware Specifications Web Site: www.nxp.com	MPC8540EC
MPC8540 PowerQUICC III™ Integrated Host Processor Reference Manual Web Site: www.nxp.com	MPC8540RM
Tsi148 PCI/X to VME Bus Bridge User Manual Web Site: www.idt.com	80A3020_MA001_02
BCM5421S 10/100/1000BASE-T Gigabit Transceiver Broadcom Corporation Web Site: www.broadcom.com	BCM5421
BCM5221S 10/100BASE-TX Single-Channel Signi-PHY Transceiver Broadcom Corporation Web Site: www.broadcom.com	BCM5221

Table A-2 Manufacturers' Documents (continued)

Document Title and Source	Publication Number
Intel 31244 PCI-X to Serial ATA Controller Datasheet Intel Corporation Literature Center 19521 E. 32nd Parkway Aurora CO 80011-8141 Web Site: http://www.intel.com/design/storage/specupdates/27379405.pdf	
Intel 31244 PCI-X to Serial ATA Controller Specification Update Intel Corporation Literature Center 19521 E. 32nd Parkway Aurora CO 80011-8141 Web Site: http://www.intel.com/design/storage/specupdates/27379405.pdf	273794-005
S29GL*xxx*N MirrorBit™ Flash Family S29GL512N, S29GL256N, S29GL128N AMD, Inc. Web Site: www.amd.com/us-en/FlashMemory	27631 Revision A Amendment 3 May 13, 2004
µPD720101 USB 2.0 Host Controller Datasheet NEC Electronics Web Site: www.necel.com/usb/en/document/index.html	S16265EJ3V0DS00 April 2003
PCI6520CB Data Book PLX Technology, Inc. Web Site: www.plxtech.com	
EXAR ST16C554/554D, ST68C554 Quad UART with 16-Byte FIFOs Web Site: www.maxlinear.com	ST16C554/554D Rev. 3.1.0
2-Wire Serial EEPROM Microchip Corporation Web Site: www.microchip.com	AT24C512
Maxim DS1621 Digital Thermometer and Thermostat Maxim Integrated Products Web Site: www.maxim-ic.com	DS1621

Table A-2 Manufacturers' Documents (continued)

Document Title and Source	Publication Number
Maxim DS1375 Serial Real-Time Clock Maxim Integrated Products Web Site: www.maxim-ic.com	Rev: 121203
TSOP Type I Shielded Metal Cover SMT Yamaichi Electronics USA Web Site: www.yeu.com	

A.3 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-3 Related Specifications

Document Title and Source	Publication Number
VITA http://www.vita.com	
VME64 Specification	ANSI/VITA 1-1994
VME64 Extensions	ANSI/VITA 1.1-1997
2eSST Source Synchronous Transfer	VITA 2.0-2003
PCI Special Interest Group (PCI SIG) http://www.pcisig.com	
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0, 2.1, 2.2	PCI Local Bus Specification
PCI-X Addendum to the PCI Local Bus Specification	Rev 1.0b
IEEE http://www.ieee.org	
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc.	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc.	P1386.1 Draft 2.0
USB http://www.usb.org/developers/docs	
Universal Serial Bus Specification	Revision 2.0 April 27, 2000