# SCP-P4040-4G-ENP2

Installation and Use

P/N: 6806800P60C

February 2020

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# About this Manual

## Overview of Contents

This manual is divided into following chapters and appendix.

*Chapter 1, Introduction on page 17* provides an overview of the product's features.

*Chapter 2, Hardware Preparation and Installation on page 23* provides instructions for installing and removing the module.

*Chapter 3, Controls, LEDs, and Connectors on page 27* provides informations on the pin assignments on the various connectors on the board

*Chapter 4, Functional Description on page 29* describes the functions of the various components on the board

*Chapter 5, Clock Structure on page 51* describes the clock distribution in the SCP-P4040-4G-ENP2. and the setup utility used to configure the product.

*Chapter 6, On-Boards Power Domains on page 53* describes the power supply system for the module.

*Chapter 7, BSP on page 55* describe how to build SCP-P4040-4G-ENP2 Basic Support Package (BSP) and deploy the built images on SCP-P4040-4G-ENP2.

*Safety Notes on page 63* lists the safety notices that are applicable to this product.

*Sicherheitshinweise on page 67* provides the German translation of the safety notes.

## Abbreviations

This document uses the following abbreviations:

| Abbreviation | Definition |
|---|---|
| AC '97 | Audio CODEC (Coder-Decoder) |
| ACPI | Advanced Configuration Power Interface - software standard to implement power saving modes in PC-AT systems |
| Basic Module | COM Express™ 125mm x 95mm module form factor |
| Carrier Board | An application specific circuit board that accepts a COM Express™ module |
| DP | Display Port |
| DVI | Digital Visual Interface |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |

| Abbreviation | Definition |
|---|---|
| GPI | General Purpose Input |
| GPIO | General Purpose Input Output |
| GPO | General Purpose Output |
| HDMI | High Definition Multimedia Interface |
| I2C | Inter Integrated Circuit - 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values |
| IDE | Integrated Device Electronics - parallel interface for hard disk drives - also known as PATA |
| LPC | Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC |
| LVDS | Low Voltage Differential Signaling - widely used as a physical interface for TFT flat panels. LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications. |
| PCI | Peripheral Component Interface |
| PCIE | Peripheral Component Interface Express - next-generation high speed Serialized I/O bus |
| PHY | Ethernet controller physical layer device |
| Pin-out Type | A reference to one of five COM Express definitions for what signals appear on the COM Express module connector pins |
| SPD | Serial Presence Detect - refers to serial EEPROM on DRAMs that has DRAM module configuration information |
| S0, S1, S2, S3, S4, S5 | System states describing the power and activity level.<br>S0 Full power, all devices powered S1 S2 S3 Suspend to RAM System context stored in RAM; RAM is in standby.<br>S4 Suspend to Disk System context stored on disk.S5 Soft Off Main power rail off, only standby power rail present. |
| SATA | Serial AT Attachment: serial-interface standard for hard disks |
| SDVO | Serialized Digital Video Output - Intel defined<br>format for digital video output that can be used with Carrier Board conversion ICs to create parallel, TMDS, and LVDS flat panel formats as well as NTSC and PAL TV outputs. |

| Abbreviation | Definition |
|---|---|
| Super I/O | An integrated circuit; typically interfaced via the LPC bus that provides legacy PC I/O functions including PS2 keyboard and mouse ports, serial and parallel port(s) and a floppy interface |
| USB | Universal Serial Bus |
| VGA | Video Graphics Adapter - PC-AT graphics adapter standard defined by IBM |
| WDT | Watch Dog Timer |

# Conventions

The following table describes the conventions used throughout this manual.

| Notation | Description |
|---|---|
| 0x00000000 | Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets |
| 0b0000 | Same for binary numbers (digits are 0 and 1) |
| **bold** | Used to emphasize a word |
| `Screen` | Used for on-screen output and code related elements or commands. `Sample of Programming used in a table (9pt)` |
| **`Courier + Bold`** | Used to characterize user input and to separate it from system output |
| *Reference* | Used for references and for table and figure descriptions |
| File > Exit | Notation for selecting a submenu |
| <text> | Notation for variables and keys |
| [text] | Notation for software buttons to click on the screen and parameter description |
| ... | Repeated item for example node 1, node 2, ..., node 12 |
| .<br>.<br>. | Omission of information from example/command that is not necessary at the time |
| .. | Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers) |
| \| | Logical OR |

| Notation | Description |
|---|---|
|  | Indicates a hazardous situation which, if not avoided, could result in death or serious injury |
|  | Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury |
|  | Indicates a property damage message |
|  | Indicates a hot surface that could result in moderate or serious injury |
|  | Indicates an electrical situation that could result in moderate injury or death |
|   | Indicates that when working in an ESD environment care should be taken to use proper ESD practices |
|   | No danger encountered, pay attention to important information |

# Summary of Changes

This manual has been revised and replaces all prior editions.

| Part Number | Publication Date | Description |
|---|---|---|
| 6806800P60C | February 2020 | Rebrand to SMART Embedded Computing template. Updated mentions of Freescale to NXP, removed Declaration of Conformity, Updated RoHS and Ordering information. Updated Safety Notes (English and German) |
| 6806800P60B | August 2014 | Re-branded to Artesyn template. |
| 6806800P60A | August 2012 | Initial Version. |

# Introduction

## 1.1 Overview

The SCP-P4040-4G-ENP2 is a COM Express module based on the NXP Power PC P40x0 platform.This board provides some of the universal interfaces such as Gigabit Ethernet, USB, PCIE, and so on.

## 1.2 Features

Following are the features of the SCP-P4040-4G-ENP2:

- Form factor: Basic (95mm x 125mm) Bullet list 2
- P4040 CPU supported
- Boot options:
  - 16 bits width NOR flash from local bus (standard product default)
  - NAND flash from local bus
  - I2C EEPROM

  **NOTE:** Selectable via carrier
- Operating system:
  - Linux
  - VxWorks

  **NOTE:** VxWorks is only a plan rather than requirement Supported CPU: P4040
- (P4040) dual channel laid down DDR3, 2GB per channel, ECC (with option to populate only one channel (top) at 2GB)
- (P4040) 16 lanes of SERDES routed to COME connectors, which can be configured as PCIE, XAUI, SRIO, SGMII
- Four UARTs or two DUARTs
- (P4040) 0/1/2 GE ports (option available to use this port as USB)
- (P4040) 5/4/0 USB ports
- 1588 signals output to the COME connectors
- Total three I2C buses
- One SPI bus with three chip select signals
- Connected from the SDHC pins to COME connectors
- Connected from the tamper detect pins to COME connectors

- Eight GPI and Eight GPO to COME connectors
- On-board RTC and WDT device
- Provide both remote and local thermal sensor
- JTAG connector on module
- Aurora testing points on module
- On-board regulators supply required voltages to devices on the module
- 12V and 5V standby power supplied to module from ATX-type (or other type) power supply through COME connectors

## 1.3 Standard Compliances

This product meets the following standards:

| Standard | Description |
|---|---|
| UL60950-1 EN 60950-1 IEC 60950-1 CAN/CSA C22.2 No 60950-1 | Safety requirements |
| CISPR 22 CISPR 24 EN55022 EN 55024 | EMC Requirements on system level |
| ENTSI EN 300 019 Series | Environmental Requirement |
| Directive (EU) 2015/863 (amending Annex II to Directive 2011/65/EU) | Directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (ROHS) |
| NEBS Standard GR-63-CORE<br>ETSI EN 300019 series | Environmental requirements |

## 1.4 Mechanical Data

The following figure shows the top and side view of the board.

*Figure 1-1 SCP-P4040-4G-ENP2 Mechanical Dimensions (Top and side views)*

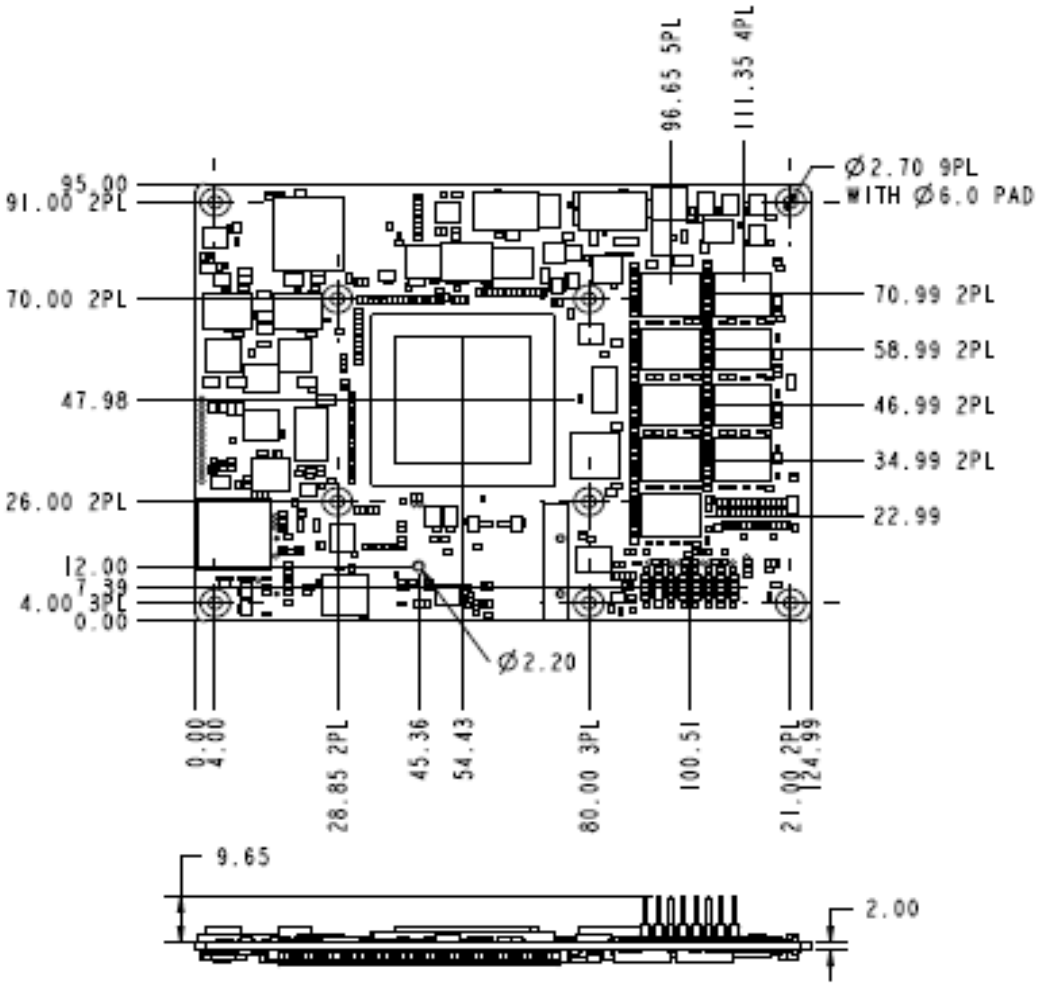


*Table 1-1 PCB Dimensions*

| Characteristic | Value |
|---|---|
| Height | 95mm |
| Length | 125mm |
| Thickness | 2mm |
| Mounting height top side (component side 1) | |
| Mounting height bottom side (component side 2) | |

# 1.5 Ordering and Support Information

This guide supports the board model listed in the following table.

*Table 1-2 Ordering Information*

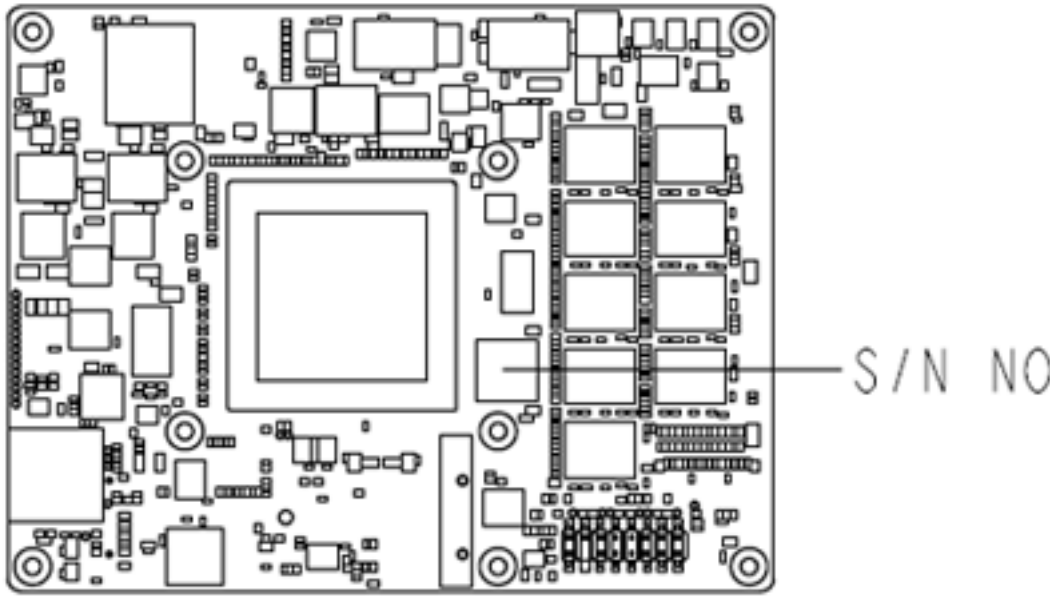
| Order Number | Description |
|---|---|
| SCP-P4040-4G-ENP2 | QorIQ P4040 with 4GB memory, ENP2. COM Express Basic size |

Consult your local SMART Embedded Computing sales representative for the availability of other variants. For technical assistance, documentation, or to report product damage or shortages, contact your local SMART EC sales representative or visit *https://www.smartembedded.com/ec/support/.*

# 1.6 Production Identification

The following figure shows the location of the board's serial number.

*Figure 1-2 Location of Product Serial Number*



# Hardware Preparation and Installation

## 2.1 Environmental and Power Requirements

You must make sure that following environmental requirements meet when board is operated in your system configuration.

**NOTICE**

**Operating temperatures refer to the temperature of air circulation around the board, but not the component temperature.**

### 2.1.1 Environmental Requirements

The following table provides the environmental requirement details for the board.

*Table 2-1 Environmental Requirements*

| Environmental Factor | Operating | Non-operating |
|---|---|---|
| Temperature | -40°C to +71°C | -50°C to +100°C |
| Humidity | to 100% RH | to 100% RH |
| Vibration Random (1hr/axis) | 0.04g2/Hz, 15 to 2000Hz (8GRMS) | |
| Shock | 30g/11mS(half sine) | |
| Altitude | -60 to 4000 m ASL | |
| Vibration Sine (10mins/axis) | 5G 15 to 2000Hz | |

### 2.1.2 Thermal Requirements

A standard passive heat sink or heat spreader can be provided by SMART EC; 12 CFM system airflow volume (at 71°C) is needed for the heat sink to keep sufficient cooling to the SCP-P4040-4G-ENP2. Contact your SMART EC sales representative for current information on the detailed thermal information of the SCP-P4040-4G-ENP2.

The following table summarized components that exhibit significant temperature raises and their maximum allowable operating temperature. These components should be monitored in order to assess thermal performance during customized thermal solution development.

*Table 2-2 Critical Temperature Spots*

| Component Identifier | Heat Dissipation Power (W) | Maximum Allowable Temperature ($^{o}$C) |
|---|---|---|
| CPU: P4040 | 16.8 | CPU: 105 (Tj) |
| GbE Transceiver: BCM5482 | 0.86 | 125 (Tj) |
| Memory SDRAM: 4GB | 3 | 95 (Tc) |

**NOTICE**

**System Overheating–Cooling Vents**

**Improper cooling can lead to system damage and an void the manufacturer's warranty. To ensure proper cooling and undisturbed airflow through the system do not obstruct the ventilation openings of the system. Make sure that the fresh air supply is not mixed with hot exhaust from other devices.**

**Personal Injury**

**During operation, hot surfaces may be present on the heat sinks and the components of the product.**

**To prevent injury from hot surface, do not touch any of the exposed components or heatsinks on the product when handling. Use the handle and face plate, where applicable, or the board edge when removing the product from the enclosure.**

## 2.1.3 Power Requirements

This board is designed to operate with the input voltages and currents as defined in the following tables.

*Table 2-3 Power Requirement (with solder-down memory chips)*

| State | 12v | VCC_RCT |
|---|---|---|
| Idle | 2.81A | 100 uA |
| Full Loading (Linux) | 2.91A | 100 uA |

*Table 2-4 Power Dissipation*

| Item | Configuration | Power |
|---|---|---|
| 1 | Total power dissipation (W) | 34.92 |

## 2.2 Unpacking and Inspecting the Board

**NOTICE**

**Damage of Circuits**

**Electrostatic discharge and incorrect installation and removal of the product can damage circuits or shorten their life.**

**Before touching the product make sure that you are working in an ESD-safe environment or wear and ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.**

1. Verify that you have received all items of your shipment:
   - Printed Quick Start Guide and Safety Notes
   - SCP-P4040-4G-ENP2 Board
   - Drivers CD
2. Check for damage and report any damage or differences to customer service.
3. Remove the desiccant bag shipped together with the product.

**NOTICE**

**Damage of Circuits–Environmental Damage**

**Improperly disposing of used products may harm the environment**

**Always dispose of used products according to your country's legislation and manufacturer's instructions.**

# 2.3 Installing and Removing the Module on the Carrier Board

The heat sink/heat spreader is already assembled with the module before these operations.

### Installing the COM module on the carrier board

1. Line up the board-to-board connector of the module assembly with the board-to-board connector of the carrier board.
2. Make sure that the inter-connectors are properly aligned and that the five standoffs on the module have contact with the top of the carrier board.
3. From the bottom side of the carrier board, locate the screw holes on module and carrier board.
4. Use the screws to fasten the module to the carrier board.

### Removing the COM module from the carrier board

1. From the back side of the carrier, locate the five screws that connect the module assembly to the carrier board.
2. Loosen and remove the screws.
3. While holding the edges, pull the module from the carrier board.

***NOTICE***

**This installation procedure is only for reference. Assemble the heatsink and the module based on your own thermal solution.**

# Controls, LEDs, and Connectors

## 3.1 Connectors and Switches

### 3.1.1 On-Board Connectors

#### 3.1.1.1 JTAG Header

The following table lists the pin-out of JTAG connector:

*Table 3-1 JTAG Connector Pin-out*

| Pin Number | Signal Name |
|---|---|
| 1 | TDO |
| 2 | NC |
| 3 | TDI |
| 4 | TRST |
| 5 | RUNSTOP |
| 6 | VDDSENSE |
| 7 | TCK |
| 8 | CKSTP INPUT |
| 9 | TMS |
| 10 | NC |
| 11 | SRST |
| 12 | NC |
| 13 | HRST |
| 14 | NC |
| 15 | CKSTP OUTPUT |
| 16 | GND |

# 3.2 On-board LEDs

There are several LEDs provided on the module to denote the statements of the system. The following table lists the LED IDs:

*Table 3-2 LED and Statements of the System*

| LED ID | Statement of the System |
|---|---|
| D17 | Thermal issue |
| D18~D19 | Debug LED 1~2 |
| D3 | System asleep |
| D7 | DDR3 power OK |
| D4 | 3.3V power OK |
| D5 | 2.5V power OK |
| D6 | 1.8V power OK |
| D13 | CORE power OK |
| D9 | PLATFORM power OK |
| D10 | 1.5V power OK |
| D1 | USB hub 1 active |
| D2 | USB hub 1 high speed |
| D15 | USB hub 2 active |
| D16 | USB hub 2 high speed |

# Functional Description

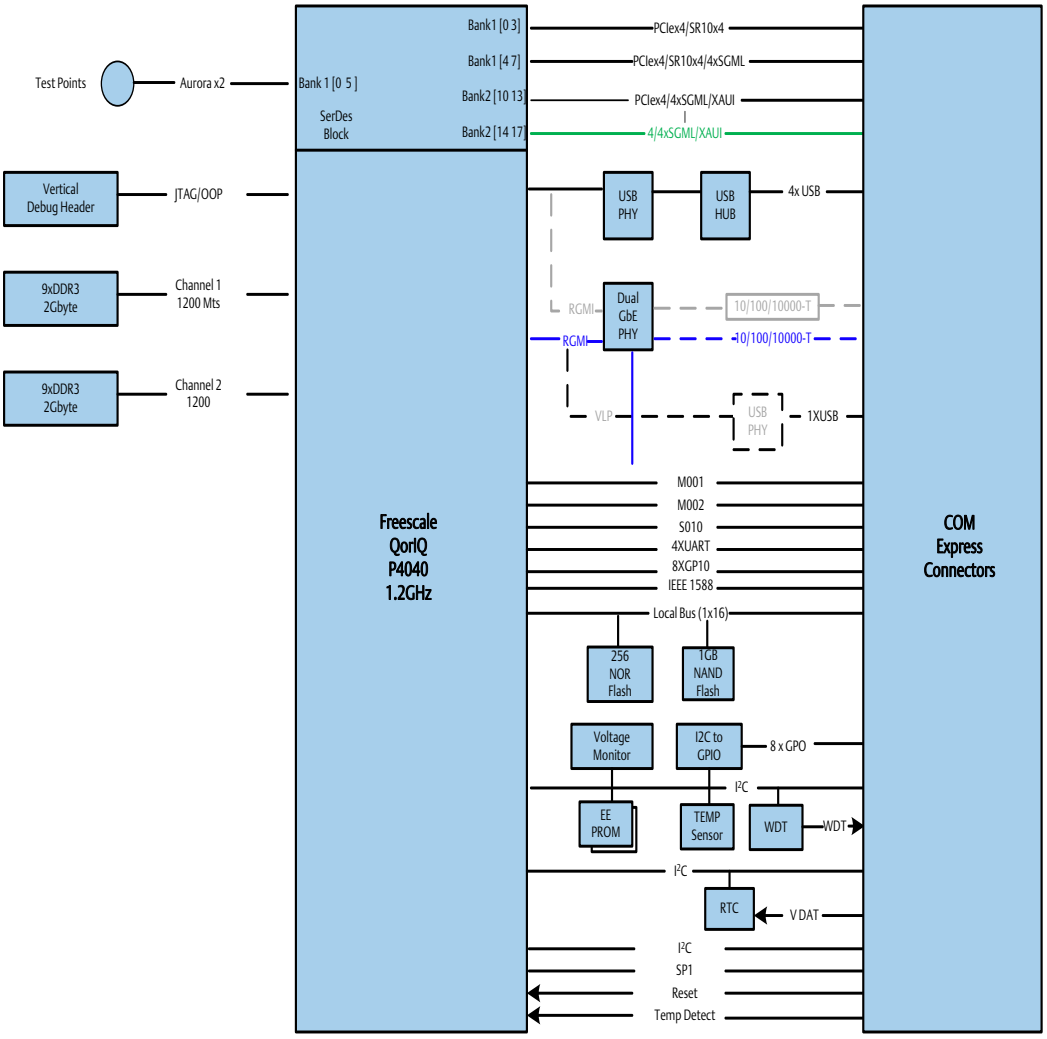
## 4.1 Overview

The SCP-P4040-4G-ENP2 is a COM Express module based on the NXP Power PC P40x0 platform.This board provides some of the universal interfaces such as Gigabit Ethernet, USB, PCIE, and so on. This board is designed to support the QorIQ P4040 integrated processor running at the speed of 1.2GHz.

The QorIQ P4040 integrated communication processor combines four Power Architecture™ processor cores with high performance data path acceleration logic, network and peripheral bus interfaces required for networking, telecommunication, data communication, wireless infrastructure, and military/aerospace applications.

# 4.2 Block Diagram

*Figure 4-1 SCP-P4040-4G-ENP2 Function Block Diagram*



## 4.3 Processor Core and Cache Memory Complex

The QorIQ P4040 has four high-performance 32-bit Power Architecture Book E-compliant e500mc cores. Each e500mc is a superscalar dual issue processor that supports out-of-order execution and in-order completion, thus making it perform better than other RISC and CISC architectures.

Features of e500mc include:

- 36-bit physical addressing
- 512-entry 4 Kbyte pages
- Three integer units (two simple, one complex)
- 1.5GHz at 1.0V
- 64 Byte cache line size
- L1 caches
- User, Supervisor, and Hypervisor instruction level privileges
- APU, classic double precision floating point unit
- 128 Kb private L2 cache running at the same frequency of CPU
- 2 Mbyte of shared L3 CoreNet platform cache (CPC)

## 4.4 Integrated Memory Controller

The P4040 consists of two DDR controllers that support DDR2 and DDR3 SDRAM. It can support a maximum of 64GByte of main memory. It is capable of ECC, detects and corrects all single bit errors, double-bit and within a nibble errors. The DDR controller is capable of self-refresh mode (for compliant DDR SDRAM DIMMs) and an initialization bypass during system power-on after an abnormal shutdown for use by designers in preventing re-initialization.

## 4.5 Local Bus

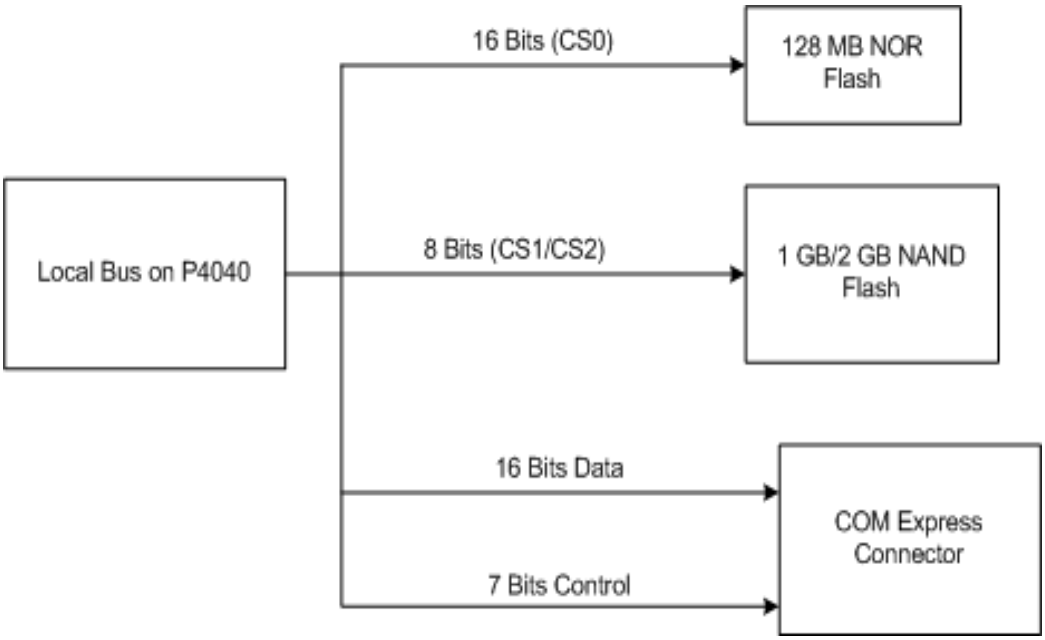
The local bus is connected to a 2Gb or 256MB NOR Flash and a 08G bits or 1G Bytes NAND flash. The NOR flash is used to store the RCW data, U-boot, and Linux kernel. By default, the NAND flash is used to store the file system. There are a totally four chip-select signals included in the local bus from CS0 to CS3. Among the CS0 to CS3, only CS0 is enabled during power on reset. So, the chip-select-signal (CS) of the device connected to local bus from which the system boots must be connected to CS0.

Local bus with 16 bits data bus (DQ0~DQ15) are directly routed to COM Express connectors.

A “low” state is required to enable local bus output and a “high” state or '1' is required to disable.

The following figure illustrates the distribution of local bus on P4040:

*Figure 4-2 Distribution of Local Bus on P4040*




## 4.5.1 Clock

The eLBC clock is generated by platform clock. The divisor is configured by CLKDIV in Clock Ratio Register (LCRR). The divisor is 32 when GPCM is selected as RCW source. So the eLBC clock is platform clock / 32 = 800MHz / 32 = 25MHz.

## 4.5.2 NOR Flash

The NOR FLASH is attached to the GPCM on local bus and works at 16-bit mode.

The NOR FLASH is Numonyx™ PC28F00 BM29EW H. Its size is 2Gb/ 256MB. It has 2048 uniform blocks, 128K bytes or 64K words each.

The physical address for NOR FLASH is 0xFE0000000 - 0xFEFFFFFFF.

The NOR FLASH should contain RCW data, u-boot image, u-boot environment variables, kernel image, device tree blob, RAMDISK image and FMAN ucode image. The detailed map is described in the following table:N

*Table 4-1 NOR Flash Map*

| Block# | Blocks | Start | End | Size | Description | Static/ Variable |
|---|---|---|---|---|---|---|
| 0 | 1 | 0000 0000 | 0001 FFFF | 128KB | Active RCW Option Data | Static |
| 1 | 12 | 0002 0000 | 0019 FFFF | 1536KB | RCW Option Data | Static |
| 13 | 3 | 001A 0000 | 0020 0000 | 384KB | Not Used | Static |
| 16 | 112 | 0020 0000 | 00FF FFFF | 14MB | FMAN ucode Image | Static |
| 128 | 1792 | 0100 0000 | 0EFF FFFF | 224MB | RAMDISK Image | Static |
| 1920 | 120 | 0F00 0000 | 0FEF FFFF | 15MB | Kernel Image | Static |
| 2040 | 3 | 0FF0 0000 | 0FF5 FFFF | 384KB | Device Tree Blob | Static |
| 2043 | 1 | 0FF6 0000 | 0FF7 FFFF | 128KB | U-Boot Env Variable | Static |
| 2044 | 4 | 0FF8 0000 | 0FFF FFFF | 512KB | U-Boot Image | Static |

### 4.5.3 NAND Flash

The NAND FLASH is attached to the FCM on local bus and works at 8-bit mode.

The NAND FLASH is Micron MT29F8G08ADADAH4 whose FLASH size is 08 G bits or 1 G Bytes. The pages are large and each page contains 2112 bytes including 2048 bytes of data and 64 bytes of spare. There are totally 8192 blocks, each block contains 64 pages including 128KB of data and 4KB of spare.

The NAND FLASH is only used as NAND FLASH JFFS2 rootfs.The detailed map is described in the following table:

*Table 4-2 NAND FLASH Map*

| Start Address | End Address | Size | Description |
|---|---|---|---|
| 0000 0000 | 00FF FFFF | 16MB | Not Used |
| 0100 0000 | 3FFF FFFF | 1GB - 16MB | NAND FLASH JFFS2 rootfs |

# 4.6 HSSI OR SERDES Block

SCP-P4040-4G-ENP2 contains SERDES 3 banks including a total of 18 lanes. From the 18 lanes of SERDES, 12 are routed to the COM Express connectors, defined as SERDES0~ SERDES7 (SERDES0~7 of bank 1) and SERDES16~SERDES19 (SERDES10~13 of bank 2). SERDES8~SERDES9 of bank 1 are used for Aurora debugger defined as Aurora0~1. The remaining 4 lanes of bank 3 are not used in P4040.

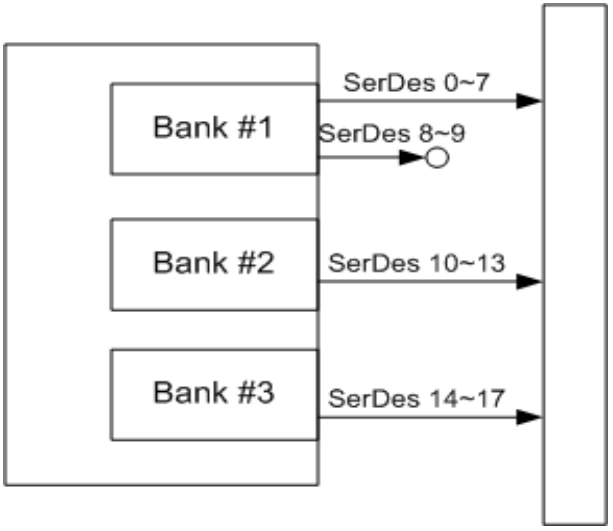
The protocol running at each lane or each group of lanes routed to COM Express connectors are configured by the RCW, available options are shown in the following table:

*Table 4-3 Options of the SERDES Routed to COM Express Connectors*

| Option # | Bank1 SerDes 0 ~ 3 (SLOT J6) | Bank1 SerDes 4 ~ 7 (SLOT J14) | Bank2 SerDes 10 ~ 13 (SLOT J10) | RCW [SRDS_ PRTCL] | Bank 3# SerDes 14~17 (slot J2) |
|---|---|---|---|---|---|
| 1 | PEX1 x4 (2.5Gbps) | PEX2 x4 (2.5Gbps) | XAUI(3.125Gbps) | 0x05 | XAUI FM1 10 GEC |
| 2 | PEX1 x4 (2.5Gbps) | PEX2 x4 (5Gbps) | XAUI(3.125Gbps) | 0x05 | XAUI FM1 10 GEC |
| 3 | PEX1 x4 (5Gbps) | PEX2 x4 (2.5Gbps) | XAUI(3.125Gbps) | 0x05 | XAUI FM1 10 GEC |
| 4 | PEX1 x4 (5Gbps) | PEX2 x4 (5Gbps) | XAUI(3.125Gbps) | 0x05 | XAUI FM1 10 GEC |
| 5 | PEX1 x4 (2.5Gbps) | SGMII x 4 (1.25Gbps) | XAUI(3.125Gbps) | 0x0F | XAUI FM1 10 GEC |
| 6 | PEX1 x4 (5Gbps) | SGMII x 4 (1.25Gbps) | XAUI(3.125Gbps) | 0x0F | Reserved[2] |
| 7 | SRIO2 x4 (3.125Gbps) | SRIO1 x4 (3.125Gbps) | PEX3 x4 (2.5Gbps) | 0x19 | Reserved[2] |
| 8 | SRIO2 x4 (3.125Gbps) | SRIO1 x4 (3.125Gbps) | PEX3 x4 (5Gbps) | 0x19 | |
| 9 | SRIO2 x4 (2.5Gbps) | SRIO1 x4 (2.5Gbps) | XAUI(3.125Gbps) | 0x13 | |
| 10 | SRIO2 x4 (3.125Gbps) | SRIO1 x4 (3.125Gbps) | SGMII x 4 (1.25Gbps) | 0x16 | |
| 11 | PEX1 x4 (2.5Gbps) | SRIO1 x4 (2.5Gbps) | XAUI(3.125Gbps) | 0x22 | |
| 12 | PEX1 x4 (5Gbps) | SRIO1 x4 (2.5Gbps) | XAUI(3.125Gbps) | 0x22 | |

The following figure illustrates the distribution of SERDES lanes on P4040:

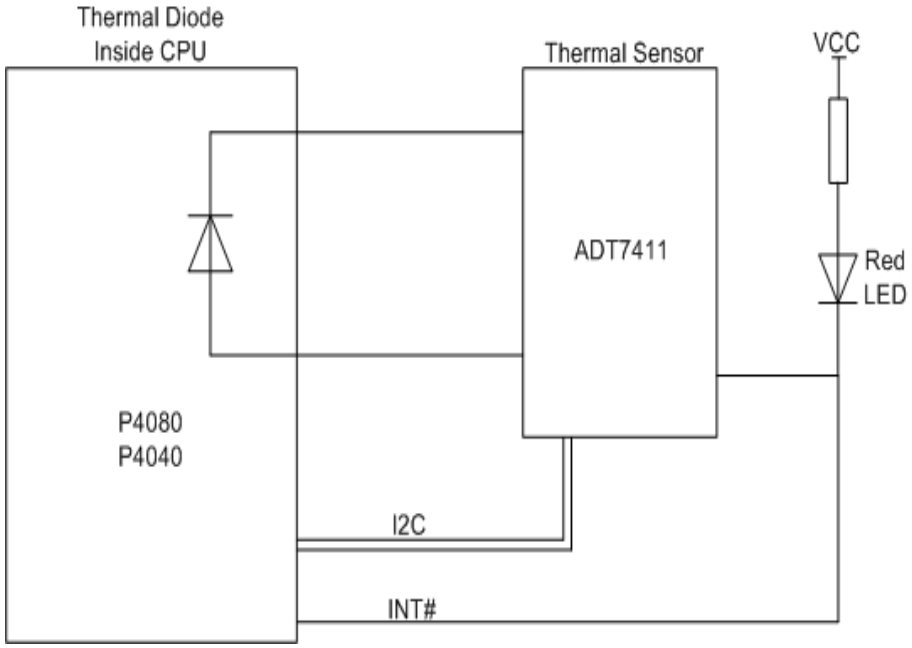
*Figure 4-3 Distribution of SERDES Lanes*



# 4.7 Thermal Management

SCP-P4040-4G-ENP2 provides a thermal management strategy.This includes CPU junction temperature monitoring. The following diagram shows thermal management strategy:

*Figure 4-4 Board Thermal Management*




A thermal diode is integrated in P40x0, which connects to a thermal sensor ADT7411. The CPU can get the junction temperature via I2C.

When the junction temperature goes up to105oC, ADT7411 drives INT# to low, indicates an interrupt to CPU. A red LED D17 can show the interrupt status.

| LED | Definition | Status | Description |
|---|---|---|---|
| D17 | INT# signal is active | ON | The CPU temperature goes up to 105°C |
| | | OFF | Normal status |

# 4.8 Main Memory

## 4.8.1 Memory Interface

QorIQ P40x0 supports two individual DDR channels that may be configured for DDR2 and DDR3. Each channel consists of 64-bit data and eight ECC bits. Both unbuffered and registered memory subsystem schemes are supported.

The module supports 4GB DDR3 1066MHz ECC memories per channel. 2GB each channel, one on top assembly and another at bottom of the PCB. Each channel contains 9x SDRAM chips on the module.

Total bottom height limit is specified as xx mm while the SDRAM's height is 1.2mm (max).

The memory interface includes all the necessary termination and I/O powers.

The following figure illustrates the DDR memory architecture per controller:

*Figure 4-5 Memory Interface*

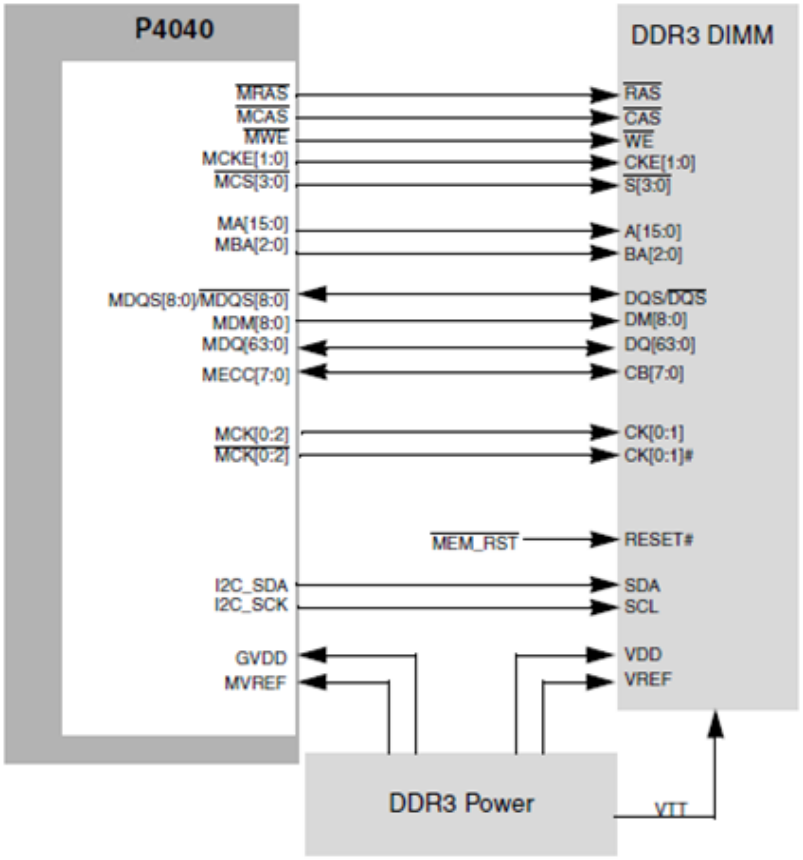



*Table 4-4 Memory Capacities*

| Characteristic | Value |
|---|---|
| Memory technology | DDR3 |
| SDRAM chip | MT41J256M8HX-15E IT:D |
| Memory Size | 2Gb 256x8 |
| Supply voltage | 1.5V |
| Oracle Number | 5106813C55 |

# 4.9 Memory Map

The following table provides the memory map of SCP-P4040-4G-ENP2.

*Table 4-5 Memory Map*

| Address # | 32-bit Effective Base Address | 36-bit Physical Base Address | Size | Description |
|---|---|---|---|---|
| 1 | 0000 0000 | 0 0000 0000 | 8000 0000 - 2GB | DDR3 Memory, NOTE1 |
| 2 | 8000 0000 | C 0000 0000 | 2000 0000 - 512MB | PCIE1 MEM |
| 3 | A000 0000 | C 2000 0000 | 2000 0000 - 512MB | PCIE2 MEM, NOTE2 |
| 4 | A000 0000 | C 2000 0000 | 1000 0000 - 256MB | RIO1 MEM, NOTE2 |
| 5 | B000 0000 | C 3000 0000 | 1000 0000 - 256MB | RIO2 MEM, NOTE2 |
| 6 | C000 0000 | C 4000 0000 | 0800 0000 - 512MB | PCIE3 MEM |
| 7 | E000 0000 | F E000 0000 | 1000 0000 - 256MB | LBC NOR FLASH |
| 8 | F000 0000 | F 0000 0000 | 0040 0000 - 4MB | DCSR |
| 9 | F400 0000 | F F400 0000 | 0020 0000 - 2MB | BMAN MEM |
| 10 | F420 0000 | F F420 0000 | 0020 0000 - 2MB | QMAN MEM |
| 11 | F800 0000 | F F800 0000 | 0001 0000 - 64KB | PCIE1 IO |
| 12 | F801 0000 | F F801 0000 | 0001 0000 - 64KB | PCIE2 IO |
| 13 | F802 0000 | F F802 0000 | 0001 0000 - 64KB | PCIE3 IO |
| 14 | FFA0 0000 | F FFA0 0000 | 0010 0000 - 1MB | NAND FLASH Buffer |
| 15 | FE00 0000 | F FE00 0000 | 0100 0000 - 16MB | CCSR |
| 16 | FFFF F000 | 0 FFFF F000 | 0000 1000 - 4KB | BOOT PAGE |

## NOTICE

**Only up to 2GB memory is mapped in u-boot and the other memory is left unmapped and not used if more than 2GB memory is fitted. More than 2GB can be used in Linux. Up to 4GB has been verified.**

**Address #4 and #5 is used instead of address #3 if RIO is configured.**

# 4.10 GPIO

SCP-P4040-4G-ENP2 consists of totally 21 GPIOs. The following table lists the GPIOs:

*Table 4-6 GPIO*

| GPIO Name | Function |
|---|---|
| CPU_GPIO0 | GPI0 of COME connectors |
| CPU_GPIO1 | GPI1 of COME connectors |
| CPU_GPIO2 | GPI3 of COME connectors |
| CPU_GPIO3 | GPI4 of COME connectors |
| CPU_GPIO4 | GPO0 of COME connectors |
| CPU_GPIO5 | GPO1 of COME connectors |
| CPU_GPIO6 | GPO3 of COME connectors |
| CPU_GPIO7 | GPO4 of COME connectors |
| CPU_GPIO19 | Clock generators enable control |
| CPU_GPIO20 | Carried board reset output |
| CPU_GPIO23 | Clock generator of bank 1 frequency selection |
| CPU_GPIO24 | Clock generator of bank 2 frequency selection |
| CPU_GPIO26 | Clock generator of bank 3 frequency selection |
| IOEXT_GPI5 | GPI5 of COME connectors |
| IOEXT_GPI6 | GPI6 of COME connectors |
| IOEXT_GPI7 | GPI7 of COME connectors |
| IOEXT_GPI8 | GPI8 of COME connectors |
| IOEXT_GPO5 | GPO5 of COME connectors |
| IOEXT_GPO6 | GPO6 of COME connectors |
| IOEXT_GPO7 | GPO7 of COME connectors |
| IOEXT_GPO8 | GPO8 of COME connectors |

GPIO18, 19, 20, 23, 24 and 26 are multiplexed with other functional blocks. The pins should be configured as GPIO in RCW data.

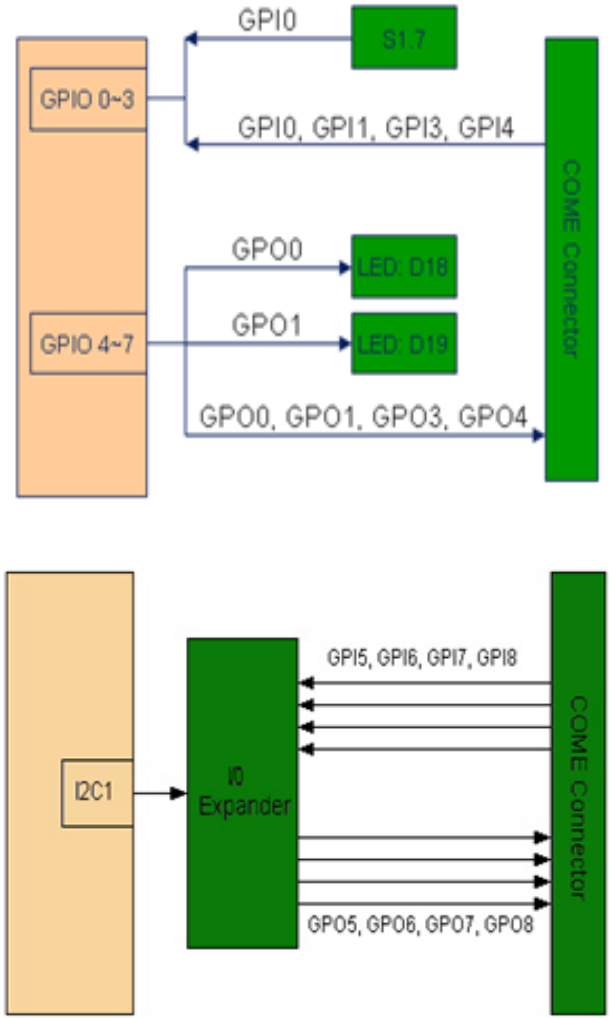
GPIO18/19: RCW [DMA1]=1b

GPIO20: RCW [DMA2]=10b

GPIO23/24/26: RCW [IRQ]=1b

After reset, the direction for all GPIOs are set to input. So all the GPIOs used as output needs to be reconfigured.

*Figure 4-6 Distribution of GPIO*



# 4.11 SDHC

SCP-P4040-4G-ENP2 provides an SD/MMC interface to the COM Express connector and there should be a SD card connector provided on the carrier.

This module not only supports SD card but also Micro SD card in which there is no write protect signal. The sixth bit of the switcher S2 is provided to define whether a SD card or Micro SD card is embedded in the carrier board.

*Table 4-7 SD or Micro SD Card on the Carrier*

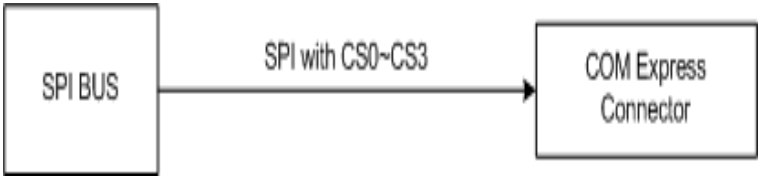
| S2.6 | Card on the carrier |
|---|---|
| ON | SD card |
| OFF (Default) | Micro SD card |

# 4.12 SPI Interface

SCP-P4040-4G-ENP2 provides a SPI bus with 3 chip-select signals. All SPI bus signals are routed to COM Express connectors.

The following figure illustrates the distribution of SPI bus:

*Figure 4-7 Distribution of SPI Bus*




# 4.13 LAN

This module provides one Gigabit Ethernet port with LED controlling signals routing to the COM Express connectors and the magnetic must be placed on carrier board. The interface used between MAC and PHY BCM5482 is the RGMII bus in P4040, which is multiplexed with USB1 ULPI bus, so RCW [EC1] should be set to 00 as RGMII protocol.

U-boot should provide the driver of dTSEC and TCP/IP protocol stack. The U-boot can use TFTP to download images to memory.

### 4.13.1 MDIO

There are totally two groups of MDIO buses in P4040. The first group is called EMI1 which complies with IEEE 802.3 Clause 22. EMI1 has two pins: EMI1_MDC and EMI1_MDIO. It is available externally only on dTSEC0@FMan1. EMI1 is used for the communication between dTSEC, MAC, and PHY. SGMII PHY is also managed by EMI1.

The second group is called EMI2 which complies with IEEE 802.3ae Clause 45. EMI2 has two pins: EMI2_MDC and EMI2_MDIO. It is available externally only on 10GEC of FMan1. EMI2 is used for the communication between 10GEC and PHY.

### 4.13.2 PHY

dTSEC0@FMan1 is connected to BCM5482 via RGMII. There are totally two ports included in the GE PHY BCM5482 and only first port is used.The MDIO address for the first port is 0x01 and the second is 0x02.

The MDIO addresses for four SGMII PHYs are 0x1C, 0x1D, 0x1E and 0x1F when SerDes option #5/#6 or #10 is applied.

## 4.14 UART Interface

SCP-P4040-4G-ENP2 consists of four UARTS (Tx and Rx signals for each UART) or two DUARTS (Tx, Rx, CTS, RTS signals for each DUART) that are routed to the COM Express connectors. Several optional resistors are provided to determine whether UARTS or DUARTS are routed.

When UARTS are routed, R383, R385, R387, and R389 are installed and R382, R384, R386, and R388 are removed, and vice versa.

***NOTICE***

**UART option is the default setting.**

# 4.15 RTC & WDT

The RTC and WDT functions provided in the module are embedded separated in two ICs, U2100 and U2101 respectively. The WDT is accessed through I2C1 bus of the processor, and the RTC is accessed through I2C2 bus, both with an address of 0xD0.The WDT triggers a reset output signal for power-on reset, and the RTC provides a 32 KHz clock output for the RTC clock input of the processor. Battery backup for the RTC is supplied by the VCC_BAT pin on the COME connectors.

*Table 4-8 Real Time Clock*

| Characteristic | Value |
|---|---|
| Vendor | ST Micro |
| Device | M41T62LC6F |
| Function | Real-time clock with alarm interrupt, programmable square wave output |
| Package | LCC8 (1.5 mm x 3.2 mm) |
| Oracle Number | 5106837C55 |

*Table 4-9 WDT*

| Characteristic | Value |
|---|---|
| Vendor | ST Micro |
| Device | M41T65Q6F |
| Function | Watchdog output |
| Package | QFN16 (3 mm x 3 mm) |
| Oracle Number | 5106837C56 |

# 4.16 USB

This module consists of one USB PHY (USB3315) and one 4-ports (USB4~USB7) USB hub (USB2514). The interface between the USB controller and USB PHY is ULPI bus, the second group of multiplexing interface RGMII/ULPI. So the RCW should be properly set for the using of the second group of ULPI bus.

The operating mode of the USB hub is configured by hardware strapping, and it can also be configured by I2C bus by changing the state of the strapping pins. Hardware strapping is the default method. The I2C bus address of the USB hub is 0x58 when configured.

By default configuration, all four USB ports of the hub are removable and all indicating signals are active high. Two LED provided on the module to indicate the operating state of the USB hub. One is hub active indicating LED and the other is hub high speed indicating LED.

*Table 4-10 USB PHY*

| Characteristic | Value |
|---|---|
| Vendor | SMSC |
| Device | USB3315C-CP-TR |
| Function | USB Transceiver (PHY) |
| Package | QFN24 (4.0mm x 4.0mm x 1.0mm) |
| Oracle Number | 5106812C21 |

*Table 4-11 USB HUB*

| Characteristic | Value |
|---|---|
| Vendor | SMSC |
| Device | USB2514Bi-AEZG |
| Function | USB Hub Controller |
| Package | QFN36 (6.0mm x 6.0mm x 1.0mm) |
| Oracle Number | 5106812C33 |

### 4.16.1 Four USB Ports

All four USB interfaces are directly connected to the COM Express connector.

All the four USB ports signals with two over current detecting signals, `USB_OC_0_1_N` and `USB_OC_2_3_N` are routed to the COM Express connectors. `USB_OC_0_1_N` is for USB0 and USB1, `USB_OC_2_3_N` is for USB2 and USB3.

## 4.17 I2C Interface

The NXP Power PC P4040 consists of four I2C buses. Among four I2C buses, the I2C3 bus is multiplexed with SDHC bus and remaining I2C buses are routed to COM Express connectors.

There is only one device attached to the second I2C bus I2C2, and there are 6 devices attached o the first I2C bus I2C1.

The following figure illustrates the distribution of the I2C buses:

*Figure 4-8 Distribution of I2C buses*

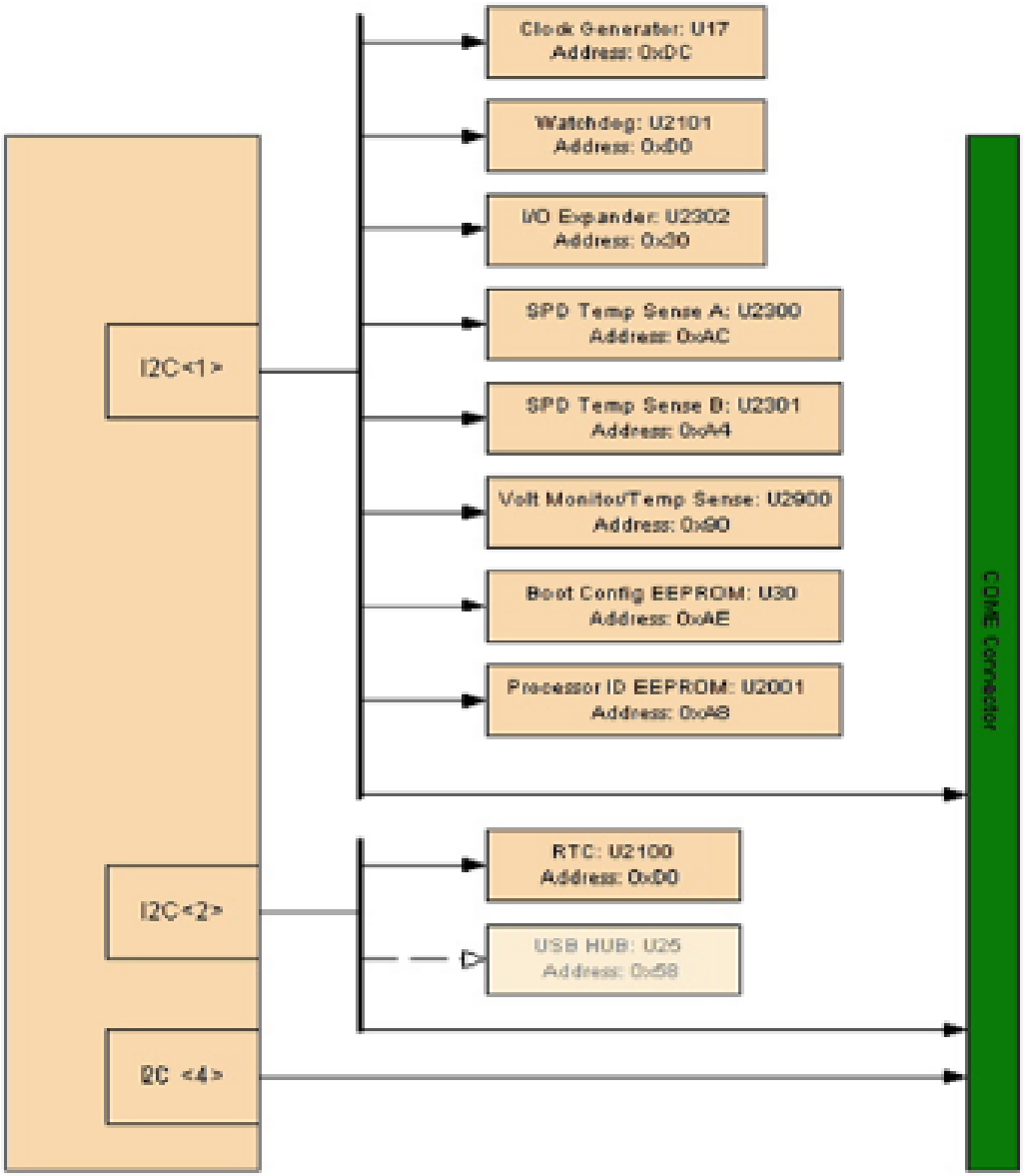


*Table 4-12 I2C Interface*

| Address | Bus | Component | Function | Oracle Number |
|---|---|---|---|---|
| 0xDC | I2C1 | 9FG104DGILFT | Clock Generator | 51NL9655W46 |
| 0xD0 | I2C1 | M41T65Q6F | Watchdog | 5106837C56 |
| 0x30 | I2C1 | PCA9557PW-T | IO-Expander | 51NL9637V06 |
| 0xAC | I2C1 | MCP98243T-BE/ST | SPD Channel A | 5106819C29 |
| 0xA4 | I2C1 | MCP98243T-BE/ST | SPD Channel B | 5106819C29 |
| 0x90 | I2C1 | ADT7411ARQZ-REEL7 | Voltage Monitor/ Temp Sense | 227975 |
| 0xAE | I2C1 | AT24C02-SSHM-T AT24C512C-SSHM-T | 2kb Boot Config EEPROM 512kb Boot Config EEPROM | 5106813C77 5106813D51 |
| 0xA8 | I2C1 | AT24C512C-XHM-T | Processor ID EEPROM | 5106813D81 |
| 0xD0 | I2C2 | M41T62LC6F | RTC | 5106837C55 |

## 4.17.1 I2C Device Thermal Sensor

The ADT7411 thermal sensor is a dual-channel digital thermometer and under/over temperature alarm. It is used in computers and thermal management systems. The ADT7411 thermal sensor is located on I2C1, U2900. The device address is 0x90. It is designed for monitoring P4040 processor temperature.

The ADT7411 can accurately measure the temperature of a remote thermal diode to ±1°C and the ambient temperature to ±3°C. The temperature measurement range defaults to 0°C to +127°C, but can be switched to a wider measurement range of-55°C to +150°C. The ADT7411 communicates over a 2-wire serial interface compatible with system management bus (SMBus) standards. An ALERT output signals when on-chip or remote temperature is out of range. The THERM output is a comparator output that allows on/off control of a cooling fan. The ALERT output can be reconfigured as a second THERM output, if required.

By default, u-boot should mask THERM and ALERT output, set the temperature measurement range from 0°C to +127°C. For setting operation mode and fetching the monitoring temperature, u-boot should provide u-boot commands.

### 4.17.2 I2C Device EEPROM

I2C device consists of two I2C EEPROMs, AT24C02C and AT24C512C. These EEPROMs are located on I2C1; one is for ID EEPROM (U30, AT24C02C, storing board serial number, MAC address and so on.) and the other is for Processor EEPROM (U2001, AT24C512C, storing processor ID and so on). The I2C addresses of these EEPROMs are 0xAE and 0xA8.

The EEPROM provides 2048 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256 words of 8 bits each.

AT24C02 support SEQUENTIAL READ and page write.

Sequential reads are initiated by either a current address read or a random address read. After micro-controller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read will continue.

AT24C02's 32K EEPROM was internally organized with 32 pages of 8 bytes each. A page write is initiated the same as a byte write, but the micro-controller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the micro-controller can transmit up to seven more data words.

### 4.17.3 I2C Device WDT

The WDT M41T65Q is located on I2C1, U2101 and the device address is 0xD0.

U-boot has the following considerations:

- By default, u-boot should mask event output and disable WDT.
- U-boot should provide commands for enabling WDT and disabling WDT.

### 4.17.4 I2C Device RTC

The RTC M41S62L is located on I2C2, U2100 and the device address is 0xD0.

U-boot has the following considerations:

- U-boot should provide commands for setting RTC date/time and getting RTC date/time.

### 4.17.5 I2C Device Clock Generator

The clock generator ICS9FG104 is located on I2C1, U17 and the device address is 0xDC.

The ICS9FG104 is a Frequency Timing Generator that provides four differential output pairs that are compliant to the Intel CK410 specification. It also provides support for PCI-Express and SATA. The part synthesizes several output frequencies from either a 14.31818MHz crystal or a 25MHz crystal. The device can also be driven by a reference clock input instead of a crystal. It provides outputs with cycle-to-cycle jitter of less than 50 ps and output-to-output skew of less than 35 ps. The ICS9FG104 also provides a copy of the reference clock.

Frequency selection can be accomplished via strap pins or SMBus control. By default, strap pins work.

For SCP-P4040-4G-ENP2, the input clock for ICS9FG104 is 25MHz and three differential output pairs are provided. First pair are connected to SerDes Bank 1, second pair are connected to x2 Aurora Connector, and third pair are connected to COM Express connector. The forth output pairs are not connected.

When using strap pins to select output frequency, SEL14M_25M# (FS3) is attached to ground (0) by option resistor. FS2 and FS1 have internal 120K pull down and the option resistors should not be soldered. FS0 is controlled by GPIO23 and S1.2. When FS0 is 0 (low level), 100MHz clock output is selected and When FS0 is 1 (high level), 125MHz clock output is selected.

### 4.17.6 I2C Device USB

I2C device consists of one USB2514 located on I2C2, U25 and the device address is 0x58.

USB2514 is a USB hub controller IC with four downstream ports for embedded USB solutions. The 4-port hub is fully compliant with the USB 2.0 Specification and will attach to an upstream port as a Full-Speed Hub or as a Full-/High-Speed Hub, and High Speed (if operating as a High-Speed Hub) downstream devices on all of the enabled downstream ports.

The SMSC Hub must be configured in order to correctly function when attached to a USB host controller. There are three principal ways to configure the hub: SMBus, EEPROM, or by internal default setting. In all cases, the configuration method will be determined by the CFG_SEL2, CFG_SEL1 and CFG_SEL0 pins immediately after RESET_N negation.

In SMBus case, the CFG_SEL1 and CFG_SEL0 pins must be 01, so that Hub can be configured as an SMBus slave for external download of user-defined descriptors.

U-boot should initialize USB hub during boot-up and provide u-boot commands for reading/writing the hub's registers.

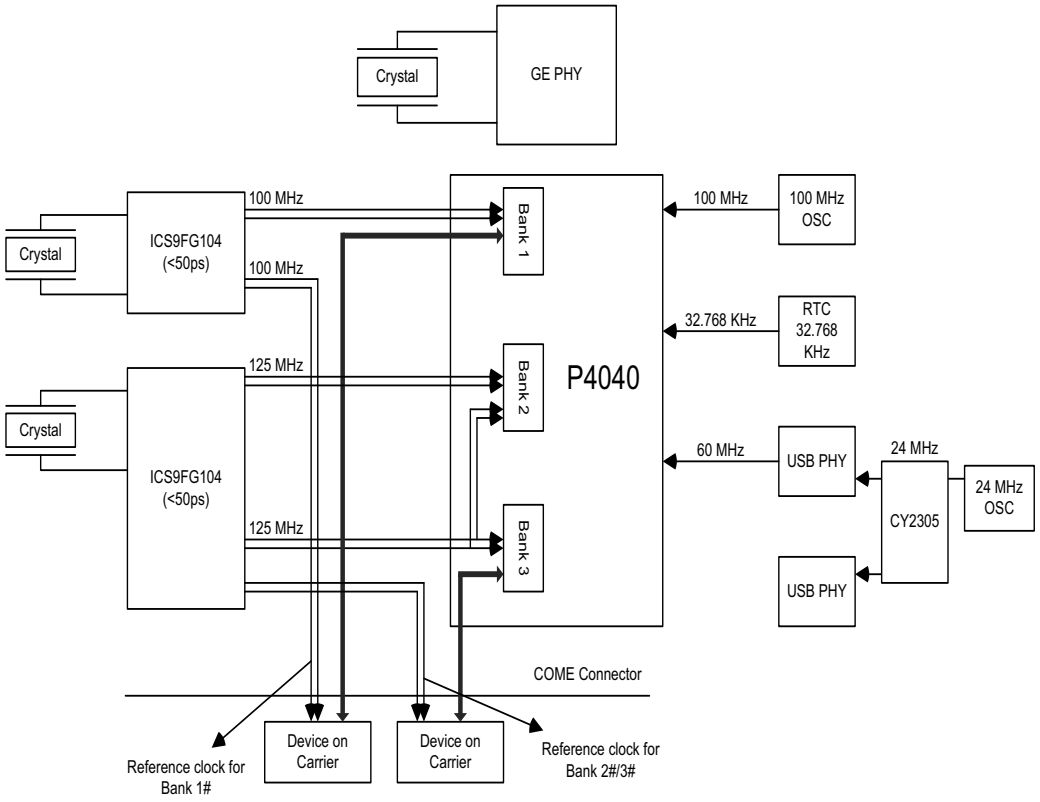
# Clock Structure

## 5.1 Overview

The SCP-P4040-4G-ENP2 needs several kinds of single ended and differential clocks for booting up and normal operating.

Following is the clock distribution tree:

*Figure 5-1 Clock Distribution*



For ruggedized variant where dip switches are not mounted, the following signals connects to COM Express connector and will be up to carrier to configure them:

| SERDES bank 1 reference clock select (pin B97 on COME) | SERDES bank 2 reference clock select (pin B98 on COME) | SERDES bank 3 reference clock select (pin B99 on COME) |
|---|---|---|
| Bank1_SEL_FS0=0, 100MHz | Bank2_SEL_S1=0, 100MHz | Bank2_SEL_S1=0, 100MHz |
| Bank1_SEL_FS0=1, 125MHz | Bank2_SEL_S1=1, 125MHz | Bank2_SEL_S1=1, 125MHz |
| *Default:100MHz | *Default:125MHz | *Default:125MHz |

For standard commercial variant where dip switches are populated, the frequency of all the three SERDES banks' reference clock is selectable between 100MHz and 125MHz by three bits of switcher S1.

| SERDES bank 1 reference clock | SERDES bank 2 reference clock | SERDES bank 3 reference clock |
|---|---|---|
| Default:100MHz | Default:125MHz | Default:125MHz |

It can also be set by three GPIOs, referring to the following table:

*Table 5-1 Configuration of the Frequency of SERDES Reference Clock by GPIO*

| SERDES bank 1 reference clock | SERDES bank 2 reference clock | SERDES bank 3 reference clock |
|---|---|---|
| CPU_GPIO23=0, 100MHz | CPU_GPIO24=0, 100MHz | CPU_GPIO26=0, 100MHz |
| CPU_GPIO23=1, 125MHz | CPU_GPIO24=1, 125MHz | CPU_GPIO26=1, 125MHz |
| Default:100MHz | Default:125MHz | Default:125MHz |

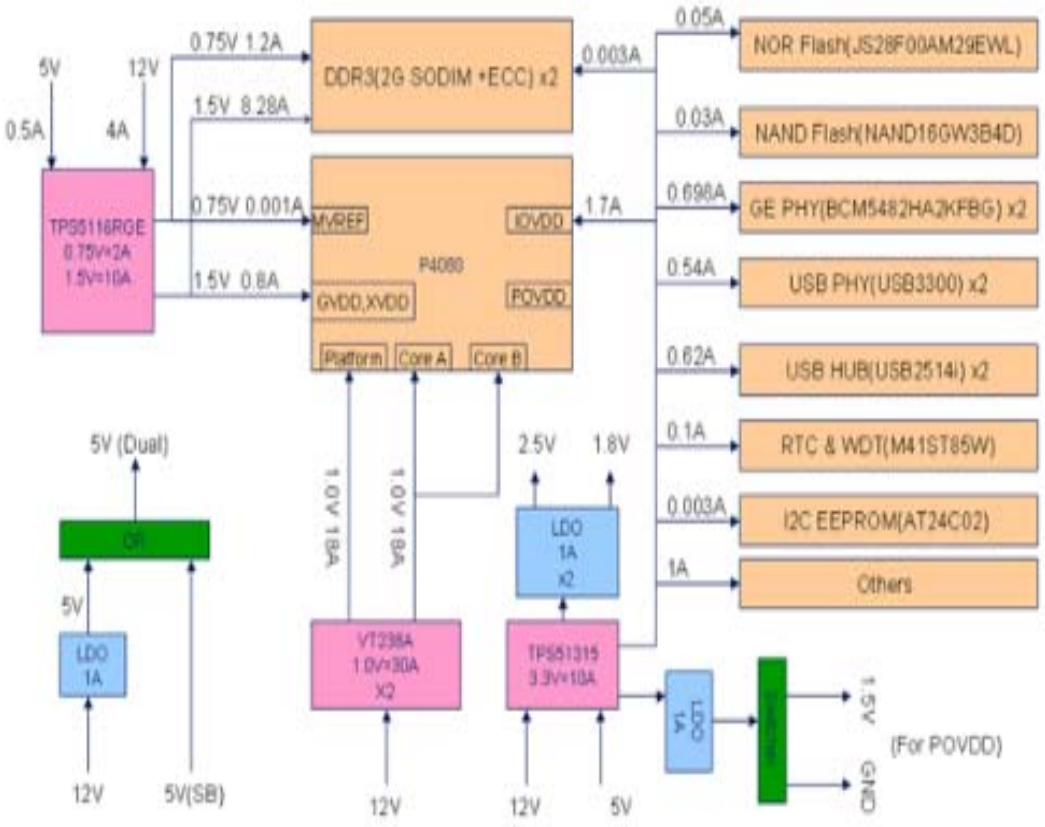
The setting of these three bits of S1 or GPIOs depends on the protocols running at the SERDES lanes of each bank. When the SERDES lanes are running at the speed of 3.125Gbps, then the corresponding bank reference clock should be set as 125MHz, and at the speed besides 3.125Gbps, it should be set as 100MHz. For example, if lanes in bank 1 are configured as PCIe, then the bank 1 reference clock should be set as 100MHz, and if XAUI, then should be set as 125MHz.

# On-Boards Power Domains

## 6.1 Overview

This subsection describes the power supply system for the module. Power is supplied to module from ATX-type (using SMART EC carrier) power supply through COM Express connectors and on-board regulators supply required voltages to devices on the module.

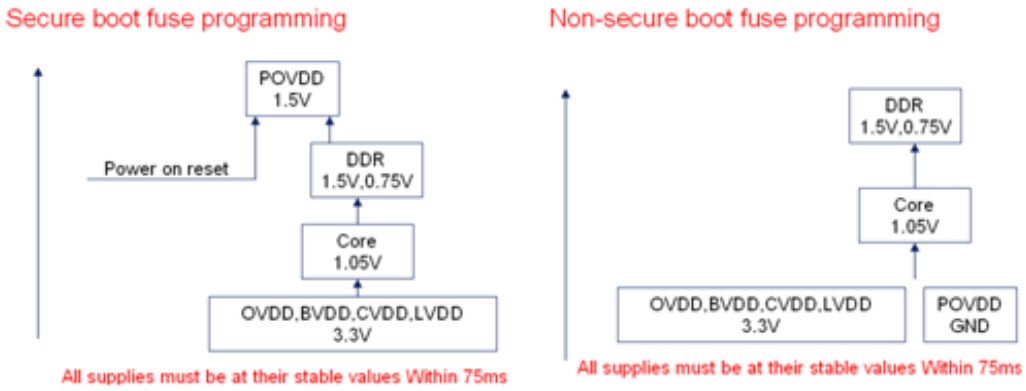
*Figure 6-1 Power Tree*



# 6.2 Power Controlling Sequence

The power sequencing of SCP-P4040-4G-ENP2 differs between secure boot mode and non secure boot mode. For secure boot mode, POVDD should be set to 1.5VDC and is powered at least 100 system clock cycles after the rising edge of power on reset signal. For non-secure boot mode, POVDD should be set to GND.

*Figure 6-2 Power Sequence of SCP-P4040-4G-ENP2*



# BSP

## 7.1 BSP Build Requirements

### 7.1.1 Build Host

The Basic Support Package (BSP) is hosted by an x86 computer running Linux. At least 1GB free space is required where the BSP is hosted.

### 7.1.2 Build Tools

Artesyn is using build tools provided in NXP SDK1.0 QorIQ-DPAA-SDK-20110609-systembuilder.iso to build BSP images for SCP-P4040-4G-ENP2.

**NOTICE**

**You can download the NXP SDK ISO files from and install it on the build host.**

### 7.1.3 Install Build Tools of SDK1.0

Following are the steps to install build tools of SDK1.0 from Freescale SDK on host computer:

1. Login to the Linux host as a non-root user, <user_name>.
2. Copy the `QorIQ-DPAA-SDK-20110609-systembuilder.iso` file to this Linux host.
3. Run the ISO file using the following command:
   ```
   sudo mount -o loop QorIQ-DPAA-SDK-20110609-systembuilder.iso /mnt/
   ```
4. Create a `/opt/freescale` directory and update access privileges using the following command
   ```
   sudo mkdir -p /unixopt/sdk1.0
   sudo chmod a+rwx /unixopt/sdk1.0
   ```
5. Change directory to mount using the following command:
   ```
   cd /mnt/
   ```
6. Install the NXP LTIB using the following commands:.
   ```
   /install
   <Input /unixopt/sdk1.0 as the installation target directory>
   ```

| NOTICE |
| --- |
| Do not interrupt the installation process. |

7. Execute the `cd /unixopt/sdk1.0/QorIQ-DPAA-SDK-20110609-system` builder command.
8. Create a PDK project for P4040DS using the following command:
   `./scripts/create-config.py --config-file=fsl-p4040ds/sample-create-config.ini`
9. Setup cross-compile environment using the `source build_p4040ds_release/bitbake.rc` command.
10. Build NXP P4040DS BSP images for building test using the `bitbake devel-image` command:

# 7.2 BSP Source Code Package

## 7.2.1 De-Compose Source Code Package

Copy the SCP-P4040-4G-ENP2 released BSP source code package `COMX_P4040_SRC_<Version Number>.tar.gz` to the build host and uncompress it in current directory:

```
tar xzvf COMX_P4040_SRC_<Version Number>.tar.gz
```

There will be a newly-created folder named p4040 which contains SCP-P4040-4G-ENP2 source code.

*Table 7-1 BSP Source Code Package Layout*

| File/Directory Name | Description |
| --- | --- |
| build.sh | Top script for building all of BSP images for BSP release. It calls Makefile to perform the operations. |
| clean.sh | Top script for cleaning all of BSP images and temporary objects for BSP release. It calls Makefile to perform the operations. |
| linux/ | linux/ directory contains Linux kernel, rootfs and rootfs building scripts. |

*Table 7-1 BSP Source Code Package Layout (continued)*

| File/Directory Name | Description |
|---|---|
| Makefile | Top makefile for building/cleaning all of BSP images for BSP release. It calls Makefiles and scripts located in sub-directories to perform the operations. |
| Makefile-p4040ds | Top makefile for building/cleaning all of BSP images for P4040DS BSP release. It calls Makefiles and scripts located in sub-directories to perform the operations. |
| misc/ | misc/ contains FMAN uCode and RCW. |
| u-boot/ | U-Boot source code. |

### 7.2.2 Setup Build Environment

If NXP SDK1.0 is used as build tool, and the host linux is 32 bit, modify the Makefile and set the environment variant PPC_TOOL_PATH as below:

```
SDK_INSTALL_PATH ?= /unixopt/sdk1.0/QorIQ-DPAA-SDK-20110609-
systembuilder
PPC_TOOL_PATH ?= $(SDK_INSTALL_PATH)/freescale-
2010.09/bin:$(SDK_INSTALL_PATH)/build_p4040ds_release/sysroots/i6
86-linux/usr/bin
```

**NOTICE**

**The build tool is not verified with SDK1.0 at 64-bit Linux host.**

## 7.3 Build BSP Images

### 7.3.1 Output Directory

By default, the output directory for building BSP images is /local/tmp/.You need to create this directory and provide full privileges for all users to access. Use the following commands to create directory and provide privileges:

```
sudo mkdir -p
sudo chmod a+rwx /local/ /local/tmp/
```

### 7.3.2 Build a Release

To build a release, run the `./build.sh <Version_Number>` command.

**NOTICE**

**The version number is formatted as VxxxAxx, VxxxBxx, VxxxTxx or VxxxRxx, for example: V100B00.**

### 7.3.3 BSP Images

SCP-P4040-4G-ENP2 BSP images should be placed in `/local/tmp/`. It includes the `COMX_P4040_<Version_Number>.tar.gz` package:

The `COMX_P4040_<Version_Number>.tar.gz` package contains:

- `comx.dtb`: Device Tree Blob
- `fsl_fman_ucode_P3_P4_P5_101_8.bin`: FMAN uCode
- `rcw.bin`: RCW
- `rcw-codewarrior.bin`: RCW used for codewarrior to burn image to NOR Flash
- `rootfs_ext2.img`: RAMDISK image
- `rootfs_nfs.tar.gz`: NFS rootfs
- `u-boot.bin`: (U-Boot)
- `uImage`: Linux kernel image

### 7.3.4 Build U-Boot

The U-Boot is based on SDK1.0 whose version is U-Boot 2011.06-rc2.

#### Commands

1. Build by default
   - `make uboot`
2. Build Targets supported for UBoot
   - `uboot`: configures and builds `u-boot.bin` for NOR flash
   - `uboot-clean`: cleans the `u-boot`

#### Output

The built image is `u-boot.bin` in the current working directory.

## 7.3.5 Build Linux Kernel

The Linux kernel is based on SDK1.0 whose version is 2.6.34.6.

### Command

1. Build by default
   - `make kernel dtb`
2. Build Targets supported for Linux kernel
   - `config-default:` copies the SCP-P4040 default configuration to current configuration
   - `kernel-config:` configures the kernel based on current configuration
   - `kernel:` compiles kernel with current configuration
   - `kernel-clean:` cleans the kernel
   - `dtb:` compiles device tree binary

### Output

The build images are uImage and comx.dtb in the current working directory.

## 7.3.6 Build ROOTFS

The rootfs for SCP-P4040-4G-ENP2 include RAMDISK and NFS.

### Commands

1. `make rootfs:` The output image is`/local/tmp/<username>/rootfs_ext2.img`
2. Build Targets supported for rootfs
   - `rootfs:` builds rootfs
   - `rootfs-ext2:` builds rootfs for ram disk
   - `rootfs-nfs:` builds rootfs for nfs
   - `rootfs-clean:` clean the rootfs

### Output

The build images are `rootfs_ext2.img` and `rootfs_nfs.tar.gz` in the current working directory.

### 7.3.7 Build Misc Firmware

Misc Firmware for SCP-P4040-4G-ENP2 includes FMAN uCode and RCW image:

- FMAN uCode is misc/fman_ucode/fsl_fman_ucode_P3_P4_P5_101_8.bin
- RCW image is misc/rcw/rcw.bin

**NOTICE**

**Both images are binary files and need not to re-build. They are copied to release package while building.**

## 7.4 DEPLOY BSP IMAGES

This section explains how to deploy BSP images. Assuming that you have built a BSP release package `COMX_P4040_V100B00.tar.gz` by running `./build.sh V100B00` located at `/local/ tmp/`.

### 7.4.1 Pre-Deployment Steps

The following steps must be performed before deployment:

1. Connect the board to your network using a network cable to the SGMII Ethernet port.
2. Setup a TFTP server in this network. Assuming that the IP address of this server is 192.168.0.100 and the root directory is `/tftpboot/`.
3. Create a `comx_p4040/ in /tftpboot/` subdirectory.
4. Copy the `COMX_P4040_<Version_Number>.tar.gz` file into the directory `/tftpboot/comx_p4040/` on TFTP server.
5. Change current directory to `/tftpboot/comx_p4040/.`
6. Unzip the.tar.gz file to the current directory. The following files are extracted to the `COMX_P4040_V100B00/`:
   - comx.dtb
   - rcw.bin
   - rcw-codewarrior.bin
   - rootfs_ext2.img
   - rootfs_nfs.tar.gz
   - uImage
   - fsl_fman_ucode_P3_P4_P5_101_8.bin
   - u-boot.bin

7. Unzip the `rootfs_nfs.tar.gz` file to the `/tftpboot/comx_p4040/` location using the `sudo tar xzvf COMX_P4040_V100B00/rootfs_nfs.tar.gz.`
8. Add `/tftpboot/comx_p4040/rootfs_nfs/` to NFS exports list in `/etc/exports:/tftpboot/comx_p4040/rootfs_nfs *(rw,sync,no_root_squash)`
9. Restart NFS service to export `/tftpboot/comx_p4040/rootfs_nfs/` using the `sudo/sbin/service nfs restart` command.
10. The following commands should be executed in U-boot command line.
11. Setup the U-Boot environment variables for the network settings. Example:

```
=> setenv ethaddr 00:01:af:12:23:01
=> setenv ipaddr 192.168.0.99
=> setenv netmask 255.255.255.0
=> setenv gatewayip 192.168.0.1
=> setenv serverip 192.168.0.100
=> setenv ethact FM1@DTSEC1
```

12. Setup the U-Boot environment variables for upgrade files. Example:

```
=> setenv rcwfile comx_p4040/COMX_P4040_V100B00/rcw.bin
=> setenv fmanfile
comx_p4040/COMX_P4040_V100B00/fsl_fman_ucode_P3_P4_P5_101_8.bin
=> setenv bootfile comx_p4040/COMX_P4040_V100B00/uImage
=> setenv norfsfile comx_p4040/COMX_P4040_V100B00/rootfs_ext2.img
=> setenv fdtfile comx_p4040/COMX_P4040_V100B00/comx.dtb
=> setenv ubootfile comx_p4040/COMX_P4040_V100B00/u-boot.bin
=> setenv rootpath /tftpboot/comx_p4040/rootfs_nfs
```

13. Test that the network and filename settings can download the files successfully. Example:

```
=> tftpboot $loadaddr $rcwfile
=> tftpboot $loadaddr $fmanfile
=> tftpboot $loadaddr $bootfile
=> tftpboot $loadaddr $norfsfile
=> tftpboot $loadaddr $fdtfile
=> tftpboot $loadaddr $ubootfile
```

## 7.4.2 Deploying BSP Images on NOR FLASH

Following are the steps to delpoy BSP images on NOR FLASH:

1. Upgrade RCW, FMAN uCode, kernel, RAMDISK image, U-Boot and DTB on NOR FLASH individually. Example:

   ```
   => run updrcw; run updfman; run updkernel; run updnorfs; run updfdt; run updubootu
   ```

2. Erase previous U-Boot environment settings using the => run eraenv command.
3. Reset the board using the => reset command. The board will boot up with new BSP.

## 7.5 RAMBOOT

Run `run ramboot` in U-Boot. ramboot will load RAMDISK, Linux kernel and DTB into RAM via network by TFTP and then boot.

## 7.6 NORBOOT

Run `run norboot` in U-Boot. norboot will load RAMDISK, Linux kernel and DTB from NOR FLASH into RAM and then boot. For details, please refer to SCP-P4040-4G-ENP2 User Manual.

## 7.7 NFSBOOT

Run `run nfsboot` in U-Boot. nfsboot will load Linux kernel and DTB into RAM via network by TFTP and then boot. And then mounting NFS on remote server as rootfs. For details, please refer to SCP-P4040-4G-ENP2 User Manual.

# Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

SMART Embedded Computing intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your SMART EC representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by SMART EC or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local SMART EC representative for service and repair to make sure that all safety features are maintained.

## EMC

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. Changes or modifications not expressly approved by SMART EC could void the user's authority to operate the equipment. Board products are tested in a representative system

to show compliance with the above mentioned requirements. A proper installation in a compliant system will maintain the required performance. Use only shielded cables when connecting peripherals to assure that appropriate radio frequency emissions compliance is maintained.

## Operation

**Product Damage**

High humidity and condensation on the board surface causes short circuits.

Do not operate the board outside the specified environmental limits.

Make sure the board is completely dry and there is no moisture on any surface before applying power.

**Damage of Circuits**

Electrostatic discharge and incorrect installation and removal can damage circuits or shorten their life.

Before touching the board or electronic components, make sure that you are working in an ESD-safe environment.

**Board Malfunction**

Switches marked as “reserved” might carry production-related functions and can cause the board to malfunction if their setting is changed.

Do not change settings of switches marked as “reserved”. The setting of switches which are not marked as “reserved” has to be checked and changed before board installation.

## Installation

**Data Loss**

Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

Make sure all software is completely shut down before removing power from the board or removing the board from the chassis.

**Product Damage**

Only use injector handles for board insertion to avoid damage to the front panel and/or PCB. Deformation of the front panel can cause an electrical short or other board malfunction.

**Product Damage**

Inserting or removing modules with power applied may result in damage to module components.

Before installing or removing additional devices or modules, read the documentation that came with the product.

## Cabling and Connectors

**Product Damage**

RJ-45 connectors on modules are either twisted-pair Ethernet (TPE) or E1/T1/J1 network interfaces. Connecting an E1/T1/J1 line to an Ethernet connector may damage your system.

- Make sure that TPE connectors near your working area are clearly marked as network connectors.
- Verify that the length of an electric cable connected to a TPE bushing does not exceed 100 meters.
- Make sure the TPE bushing of the system is connected only to safety extra low voltage circuits (SELV circuits).

If in doubt, ask your system administrator.

## Battery

**Board/System Damage**

Incorrect exchange of lithium batteries can result in a hazardous explosion.

When exchanging the on-board lithium battery, make sure that the new and the old battery are exactly the same battery models.

If the respective battery model is not available, contact your local Emerson sales representative for the availability of alternative, officially approved battery models.

**Data Loss**

Exchanging the battery can result in loss of time settings. Backup power prevents the loss of data during exchange.

Quickly replacing the battery may save time settings.

**Data Loss**

If the battery has low or insufficient power the RTC is initialized. Exchange the battery before seven years of actual battery use have elapsed.

### PCB and Battery Holder Damage

Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent damage, do not use a screw driver to remove the battery from its holder.

## Environment

### Environmental Damage

Improperly disposing of used products may harm the environment.

Always dispose of used products according to your country's legislation and manufacturer's instructions.

# Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

SMART Embedded Computing ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem Produkt in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von SMART EC.

Das System erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch SMART EC ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von SMART EC. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

## EMV

Das Produkt wurde in einem SMART EC Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse B gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse B. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Produktes in Gewerbe- sowie Industriegebieten gewährleisten.

Das Produkt arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Wird das Produkt in einem Wohngebiet betrieben, so kann dies mit grosser Wahrscheinlichkeit zu starken Störungen führen, welche dann auf Kosten des Produktanwenders beseitigt werden müssen. Änderungen oder Modifikationen am Produkt, welche ohne ausdrückliche Genehmigung von SMART EC durchgeführt werden, können dazu führen, dass der Anwender die Genehmigung zum Betrieb des Produktes verliert. Boardprodukte werden in einem repräsentativen System getestet, um zu zeigen, dass das Board den oben aufgeführten EMV-Richtlinien entspricht. Eine ordnungsgemässe Installation in einem System, welches die EMV-Richtlinien erfüllt, stellt sicher, dass das Produkt gemäss den EMV-Richtlinien betrieben wird. Verwenden Sie nur abgeschirmte Kabel zum Anschluss von Zusatzmodulen. So ist sichergestellt, dass sich die Aussendung von Hochfrequenzstrahlung im Rahmen der erlaubten Grenzwerte bewegt.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

## Betrieb

### Beschädigung des Produktes

Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Produktes können zu Kurzschlüssen führen.

Betreiben Sie das Produkt nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Produkt kein Kondensat befindet.

### Beschädigung von Schaltkreisen

Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.

Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

### Fehlfunktion des Produktes

Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.

Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ggf. ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Produkt installieren.

## Installation

**Datenverlust**

Das Herunterfahren oder die Deinstallation eines Boards bevor das Betriebssystem oder andere auf dem Board laufende Software ordnungsmemäss beendet wurde, kann zu partiellem Datenverlust sowie zu Schäden am Filesystem führen.

Stellen Sie sicher, dass sämtliche Software auf dem Board ordnungsgemäss beendet wurde, bevor Sie das Board herunterfahren oder das Board aus dem Chassis entfernen.

**Beschädigung des Produktes**

Fehlerhafte Installation des Produktes kann zu einer Beschädigung des Produktes führen.

Verwenden Sie die Handles, um das Produkt zu installieren/deinstallieren. Auf diese Weise vermeiden Sie, dass das Face Plate oder die Platine deformiert oder zerstört wird.

**Beschädigung des Produktes und von Zusatzmodulen**

Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Produktes und der Zusatzmodule führen.

Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

## Kabel und Stecker

**Beschädigung des Produktes**

Bei den RJ-45-Steckern, die sich an dem Produkt befinden, handelt es sich entweder um Twisted-Pair-Ethernet (TPE) oder um E1/T1/J1-Stecker. Beachten Sie, dass ein versehentliches Anschließen einer E1/T1/J1-Leitung an einen TPE-Stecker das Produkt zerstören kann.

- Kennzeichnen Sie deshalb TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes deutlich als Netzwerkanschlüsse.
- Stellen Sie sicher, dass die Länge eines mit Ihrem Produkt verbundenen TPE-Kabels 100 m nicht überschreitet.
- Das Produkt darf über die TPE-Stecker nur mit einem Sicherheits-Kleinspannungs-Stromkreis (SELV) verbunden werden.

Bei Fragen wenden Sie sich an Ihren Systemverwalter.

## Batterie

**Beschädigung des Blades**

Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.

**Datenverlust**

Wenn Sie die Batterie austauschen, können die Zeiteinstellungen verloren gehen. Eine Backupversorgung verhindert den Datenverlust während des Austauschs.

Wenn Sie die Batterie schnell austauschen, bleiben die Zeiteinstellungen möglicherweise erhalten.

**Datenverlust**

Wenn die Batterie wenig oder unzureichend mit Spannung versorgt wird, wird der RTC initialisiert.

Tauschen Sie die Batterie aus, bevor sieben Jahre tatsächlicher Nutzung vergangen sind.

**Schäden an der Platine oder dem Batteriehalter**

Wenn Sie die Batterie mit einem Schraubendreher entfernen, können die Platine oder der Batteriehalter beschädigt werden.

Um Schäden zu vermeiden, sollten Sie keinen Schraubendreher zum Ausbau der Batterie verwenden.

## Umweltschutz

Falsche Entsorgung der Produkte schadet der Umwelt.

Entsorgen Sie alte Produkte gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.